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JOULE HEATING INDUCED INTERCONNECT FAILURE IN 3D IC TECHNOLOGY

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Menglu Li

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ABSTRACT OF THE DISSERTATION

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Professor King-Ning Tu, Chair

With the slow-down of Moore's law of scaling transistors, the industry is looking for 3D IC technology to extend the Moore's law by stacking chips vertically. In the 3D IC technology, Joule heating is the most serious reliability concern because of increased power density. Moreover, there are new interconnects in the package to support vertical stacking, including the Through Silicon Via (TSV) inside silicon die, μ-bumps between different dies, and redistribution layer (RDL) to fan out the current between μ-bumps and TSVs, and between TSV and flip chip solder joints. Thus, how does joule heating affect the reliability of the new interconnects is of most interest. In this thesis, we applied the electromigration test to induce joule heating in our packaging system, and studied the weak link of the 3D IC system first. It is found that the redistribution layer is the weak link and failed by burn-out voids. The failure

mode is evaluated by finite element analysis and found to be joule heating enhanced electromigration. Then, we optimized the redistribution design in the power delivery system to reduce the thermal effect and minimize the IR drop (covered in Chapter 3). It is found that an optimal power distribution system requires larger TSVs integrated at the super fat capture levels (RDL), rather than small TSVs captured at the lower levels. We further evaluated the electromigration resistance of optimized RDL and found that fat wire can pump more current but the surface treatment of Cu RDL limits the maximized current. In Chapter 4, we found that the lateral joule heating transfer through Si interposer will induce high enough temperature gradient inside the un-powered microbumps next to the powered microbumps, and fail the un-powered microbumps by thermomigration. The heat transfer creates a large temperature gradient, in the order of 1000 ^{o}C/cm, through the un-powered microbumps in the neighboring chip, so the microbumps failed by thermomigration. In our test structure, we have found other microbumps which were failed by electromigraion as well as by constant temperature annealing. We used synchrotron radiation tomography to compare the failure in these three kinds of microbumps: microbumps under electromigration, microbumps under thermomigration, and microbumps under a constant temperature thermal annealing. The results show that the microbumps under thermomigration have the largest damage. Our calculations showed that indeed the electromigration and thermomigration driving force are in the same order. The latter induced atomic flux of Sn to go from the cold end to the hot end, resulting in depletion and void formation at the cold end. Furthermore, the temperature gradient tends to enhance sidewall surface diffusion of Sn to react with Ni and Cu. This sidewall surface diffusion of Sn can cause significant void formation in the solder layer in the microbumps.

The dissertation of Menglu Li is approved.

Subramanian Srikantes Iyer

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King-Ning Tu, Committee Chair

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This thesis is dedicated to our beloved daughter, Lori Ye.

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1. Li, M., Kim, D.W., Gu, S., et al, 2016. Joule heating induced thermomigration failure in un-powered microbumps due to thermal crosstalk in 2.5D IC technology. Journal of Applied Physics. (submitted).
2. Li, M., Periasamy, P., Iyer, S.S., Tu, K.N., 2016. Electrical-thermal analysis of the optimized power delivery for 3D Integration by using grind-side redistribution layer. IEEE Transactions on CPMT. (drafted).
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4. Liu, Y., Li, M., Kim, D.W., Gu, S. and Tu. K.N., 2015. Synergistic effect of electromigration and Joule heating on system level weak-link failure in 2.5 D integrated circuits. Journal of Applied Physics, 118(13), p.135304.

Chapter 1 Introduction

1.1 Three-Dimensional Integrated Circuits (3D IC) Technology

As Moore's law is slowing down beyond 14nm node technology, due to significant challenge in materials, process complexity, and manufacturing cost [1-3], the semiconductor industry is developing technologies to extend Moore's law, so called "More than Moore" technologies. 3D IC technology, by stacking chips vertically, is one of the promising packaging technologies to continue Moore's law. Fig.1.1 is the schematic and SEM cross-section image to show 3D IC technology. In order to make vertical connections between stacking chips, through silicon via (TSV) and microbumps (μ-bump) as indicated in Fig. 1.1, are the new interconnects in this structure. Typically, TSV is cylindrical and has a diameter of 5 μm and a height of 50 μm while μ-bump has a diameter between 20 to 40 μm and the industry is pushing towards 5 μm. The TSV is made of Cu while μ-bump is Sn based solder. After reflow (re-melting of solder) , the materials in the solder layer of μ-bump will transformed to mostly intermetallic compound (IMC). Also, if there is a number difference between different level interconnects, there is always a redistribution (RDL) wiring system to fan-out or fan-in current. For example, in Fig. 1.1, one RDL level was added between TSVs and μ-bumps to fan out current to the higher level. The RDL is made by hierarchical Cu wiring system. The thickness of Cu line and via is typically less than 1 μm. In order to mitigate the chip-package interaction (CPI), a thin Si interposer (~50 μm) is often used above the packaging laminate. If there is no device on the Si

interposer, and only one chip stacked above, then we call it 2.5D IC. If there is device on the Si interposer, or there are more chips stacked above it, we call it 3D IC.

Although the manufacturing process for the TSV and μ-bumps are becoming mature in the past ten years due to the development of Bosch technology[4] for TSV, and thermal compression bonding technology[5] for μ-bumps, the reliability study of 3D IC structure is not extensive yet[6]. The reason is due to limited 3D IC products in the market, and lack of reliability data. Consequently, we have limited knowledge on the failure mode when the structure is under power. Nevertheless, the new reliability concern based on the new structure and materials of 3D IC has been discussed. For example, the use of thin Si die for both chips and interposer will create warpage issue and handling difficulty; the stacking of multiple dies vertically will make vertical heat dissipation difficult; the large CTE mismatch of Si and Cu will create stress around TSV which might serve as crack initiation point, the IMC dominant μ-bump will be mechanically brittle, and so on. Among all of them, joule heating is the key to make all the reliability issues worse. The increased heat generation due to high power density will create thermal stress issue, such as warpage and crack. More importantly, besides the mechanical reliability, the electrical reliability, such as electromigration (EM) and thermomigration are also critical for the lifetime of the devices. For the traditional packaging interconnect, such as flip chip solder joint, Cu interconnects and Al interconnects, the electromigration resistance and failure mode is critical and limits the maximum current; and thermomigration (atomic diffusion driven by temperature gradient, and Soret effect) is occurred during EM test. The thermomigration reliability is especially important for the alloy or the intermetallic compound (IMC), which have more than one element. In this thesis, the joule heating effect on electromigration and

thermomigration of 2.5D IC has been studied. In order to couple joule heating effect in our study, all the tests are based on electromigration (EM) set up, where sufficient current is powered.

1.2 Introduction to Electromigration

Electromigration is an enhanced directional mass flow along the electron flow direction under high current density, above 10^4 A/cm^2[7-11]. The threshold current density for the EM to occur depends on different materials. Typically, Cu is on the order of 10^5 A/cm^2, Al is on the order of 10^6 A/cm^2, and Sn is on the order of 10^4 A/cm^2. Huntington model [12] describes the electromigration kinetics, as shown in Fig. 1.2. In this figure, a high current was flowed in an Al interconnect. When there is a high density of electron moving from the cathode to the anode, the momentum exchange between electrons and atoms will push atoms to move along the same direction as the electrons. This directional mass transportation will cause extrusion (hillock) at the anode side, and depletion (void) at the cathode side. The hillock and void formation will cause circuit malfunction because of possible open/short failure. The driving force is described as electron wind force. Atomically, the electrons will first move the atom to an activated state, then the atom will be further driven to the vacant state, and complete one atomic jump[13], as shown in Fig. 1.3. Aside from electron wind force, there is another force that against electromigration – back stress. Back stress is time dependent, and can be modeled as "rigid box model"[14,15]. For example, the Al interconnect is surrounded by Al_2O_3, and if we assume that this native oxide is a "rigid box", the mass flow to the anode will create a compression stress while the cathode will have tensile stress. This stress gradient will drive the atoms to

move against the electron flow direction, and balance the electromigration effect. When the interconnect is below the critical length, there is no more EM damage. The atomic flux with the consideration of both electron wind force and back stress can be described in equation 1.1[15],

$$J_{EM}^{total} = -CD\Omega\frac{\frac{d\sigma}{dx}}{kT} + CD\frac{Z^*eE}{kT} \quad \text{--- (1.1)}$$

where J_{EM}^{total} is the total atomic flux induced by EM, C (=1/Ω in a pure metal, Ω is the atomic volume) is the concentration of atoms per unit volume, D is the effective diffusivity at the testing temperature, Z^* is the effective charge number, dσ/dx is the back-stress gradient along the electron flow path, E is the electric field, where E = ρj, and ρ is the resistivity, and j is the applied current density, and k and T are Boltzmann's constant and temperature, respectively.

EM is a diffusional process, there is typically three main diffusion path for different materials: surface diffusion, grain boundary diffusion, and lattice diffusion, as shown in Fig. 1.4[16]. At the device working temperature, around 100 ℃, Al interconnect is grain boundary diffusion dominated, Cu interconnect is surface diffusion dominated, while lead-free solder is lattice diffusion dominated. A continuous and directional flux will not cause failure until there is flux divergence. Flux divergence means that the incoming atomic flux is unequal to the outgoing atomic flux, so there is atomic accumulation or the void growth at the flux divergence region. Typically, the triple point at the grain boundaries and the interphase interfaces between different materials are the main flux divergence region. For example, Al interconnect usually will reveal failure at the triple points of grain boundary, and Cu

interconnects will reveal failure at the interface between via and Cu line, or Cu surface[17,18]. But for lead-free solder (Sn based), the failure mode by EM is pancake shape (Fig. 1.5) when current take turns from the thin under bump metallization (UBM) to the ball-shape solder. For solder joints, the failure is related to geometry also. When the current take turns from the UBM to the solder joint, there is current crowding at the transition corner, as shown in Fig. 1.6(a). This current crowding effect will create an electrical potential gradient force (Fig. 1.6(b)) to drive vacancies to the low current density region, and the void will nucleate there. The constant feeding of vacancies to the void due to EM depletion of solder will enable the void to grow as a pancake shape under the UBM [19]. Therefore, current crowding effect is serious for solder joint, and it explains the failure mode.

To summarize, the electron wind force drives the atom to move directionally toward the cathode, and the flux divergence along the diffusion path will cause EM failure (void and extrusion). When there is current crowding effect, the current density gradient will drive vacancies to the low current density region, and the void will start to nucleate when the super-saturation of vacancies occurs

1.3 Introduction to Thermomigration

Thermomigration (TM) is the phenomenon of atomic diffusion driven by a temperature gradient. Mathematically, the driving force of thermomigration can be expressed in equation 1.2,

$$\mathrm{F} = -\frac{Q^*}{T}\left(\frac{\partial T}{\partial x}\right) \qquad \text{---(1.2)}$$

Where Q^* is the heat of transport, which is defined by the difference between heat carried by a moving atom per mole to the heat of atoms per mole at the initial state (the hot end or the cold end), T is the working temperature, and $\frac{\partial T}{\partial x}$ is temperature gradient. The atomic flux due to the presence of thermomigration could be expressed as [20]:

$$\mathrm{J} = \mathrm{C}\frac{D}{kT}\frac{Q^*}{T}\left(-\frac{\partial T}{\partial x}\right) \quad \text{---(1.3)}$$

Where C is the atomic concentration, and D is the diffusivity of the diffusing atom at the working temperature.

Thermomigration was usually coupled with electromigration together in the powered flip chip solder joint. In order to separate the two effects, Hsiao and Chen[21] used AC current to power the daisy chain of the solder joint (Pb-free). Before powering, FIB etched holes were used to make markers inside the solder joint. In this case, EM will not occur, but joule heating was there and will create a temperature gradient. After current stressing, the marker was moved from the cold end to the hot end (Fig. 1.7), which indicated that Sn was driven to hot end under the temperature gradient. In order to verify quantitatively the driving force, IR measurement was taken during power stressing to monitor the temperature gradient. It was found that the temperature gradient was in the order of 1000 ℃/cm, as seen in Fig. 1.8. The literature agrees that the threshold temperature gradient for TM phenomenon is indeed on the order of 1000 ℃/cm[22-25]. This means for a microbumps with 10μm height, 1 ℃ difference across the height will have thermomigration. This temperature

difference is very small. Therefore, thermomigration is a critical reliability for 3D IC technology.

1.4 Introduction to Synchrotron X-ray Micro-Tomography

In this study, 3-D images of 3D IC sample (microbumps, TSVs, ect.) before and after the electromigation tests were obtained by using 3-D synchrotron X-ray micro-tomography facility at the Advanced Light Source of Lawrence Berkeley Laboratory, Beamline 8.3.2. High-resolution 3-D X-ray tomography is a nondestructive technique for visualizing the features inside the solid. Fig. 1.9 shows a schematic of the end station of the facility. The sample is mounted on a rotation state. An X-ray energy of 35 keV was used, and 1025 images were collected as the sample was rotated over 180 degrees. A 50 micron LuAG scintillator was used with a 10x lens in an optical system from Optique Peter, with a PCO.edge camera, yielding a pixel size of 0.65 microns/pixel. The tomographic reconstruction was carried out using Octopus, and visualization and analysis was carried out in the FIJI/ImageJ and Avizo software packages. This technique is very helpful when the sample quantity (e.g. the number of TSV and μ-bump on a Si chip) is large to statistically verify the phenomenon. Also, for high aspect ratio TSV, this technique is helpful because polishing this kind of sample is very difficult.

1.5 Dissertation Outline

The 3D IC structure brings new reliability issue. Among them, the most critical

one is joule heating [26]. Because 3D stacking increased the power density, and decreased the heat dissipation capability by using thin die and underfill in between. The heat dissipation is very critical. If heat is not dissipated away effectively, then the local hot spot will create new failure mode with respect to electromigration tests. Chapter 2 will discuss this topic thoroughly. In Chapter 3, based on the failure mode and system weak link, we optimized the redistribution design to improve the power delivery, and we also evaluated this redistribution design by simulation and experiment. In Chapter 4, we will discuss the thermal cross talk induced failure in the un-powered microbumps. Because of the use of Si interposer on the organic substrate, the horizontal joule heating transfer through Si interposer will cause thermal cross-talk between different dies above. This phenomenon is illustrated in Fig. 1.10. Chapter 5 is a summary of the findings.

1.6 Figures

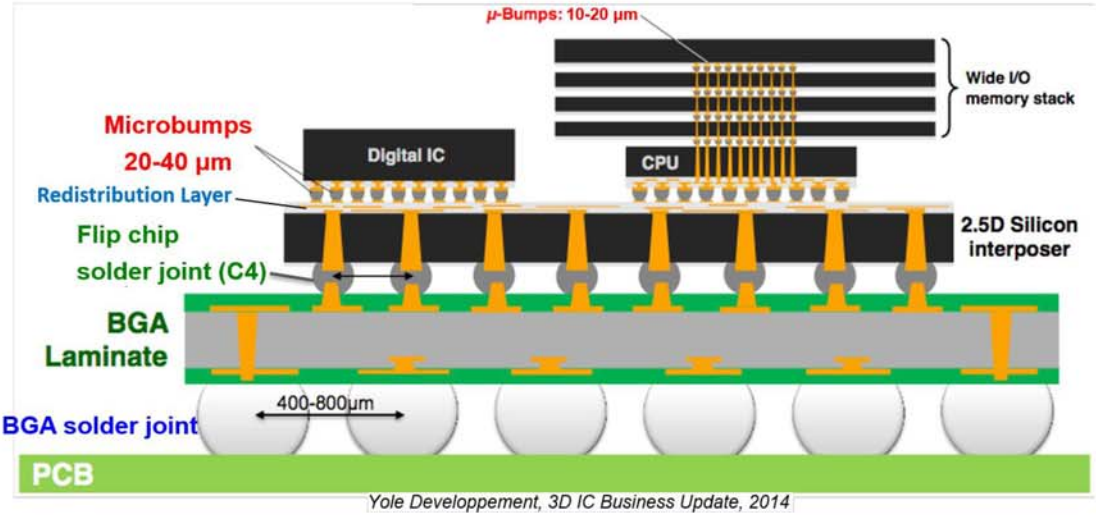

Figure 1.1 Schematic of 3D IC packaging

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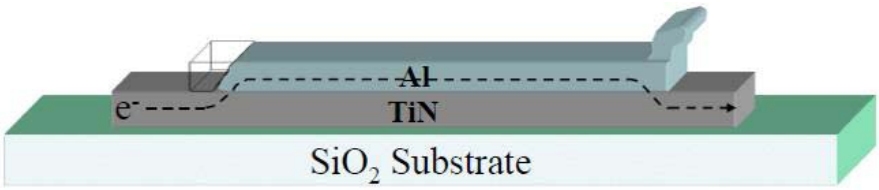


Figure 1.2 Huntington model of electromigration driving force.

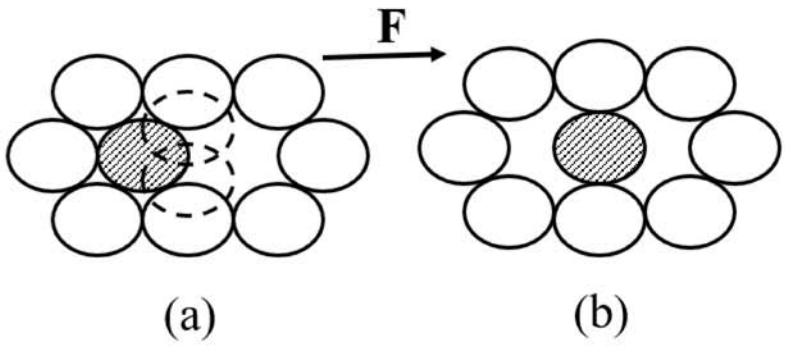
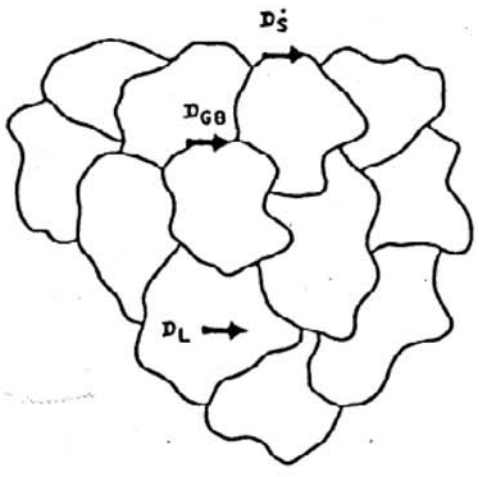


Figure 1.3 Atomic jump driving by EM force.



D_S surface diffusion
D_{GB} grain boundary diffusion
D_L lattice diffusion
For Al $D_{GB} >> D_s$ or D_L

Figure 1.4 Different diffusion paths in solid.

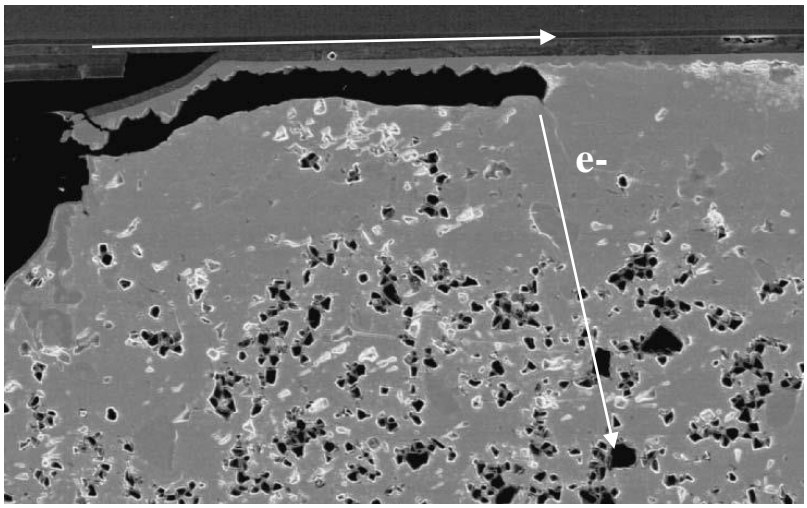


Figure 1.5 Electromigration induced pancake void formation in the flip chip solder joint

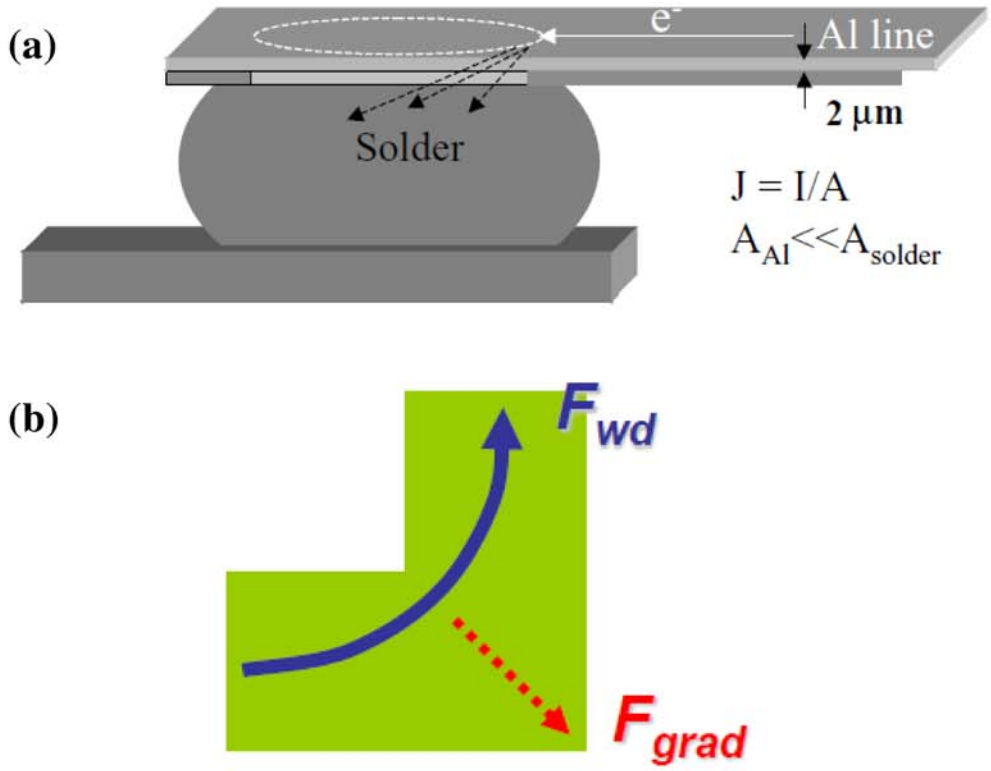


Figure 1.6 Schematic showing (a) current crowding phenomenon; (b) electrical potential gradient force.

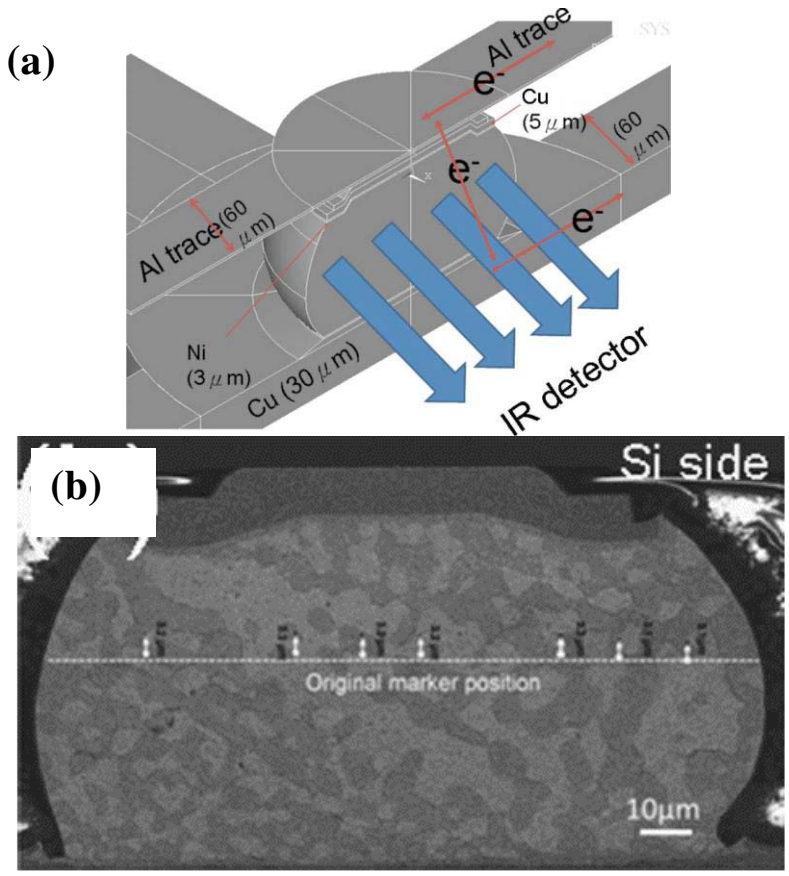


Figure 1.7 Thermomigration phenomenon by applying AC current. (a) Experimental set-up; (b) Marker movement after test

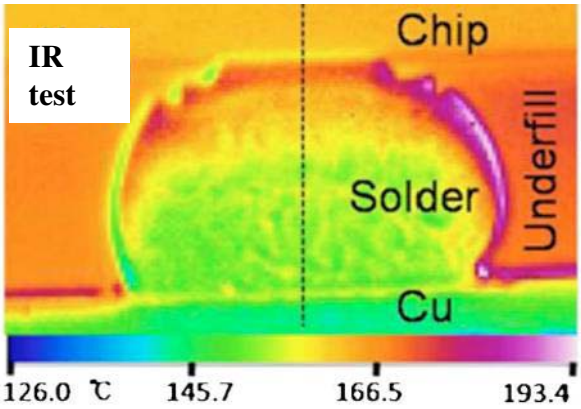


Figure 1.8 IR measurement of the temperature distribution of the solder under TM test; $\frac{\Delta T}{\Delta x}$ =2571℃/cm.

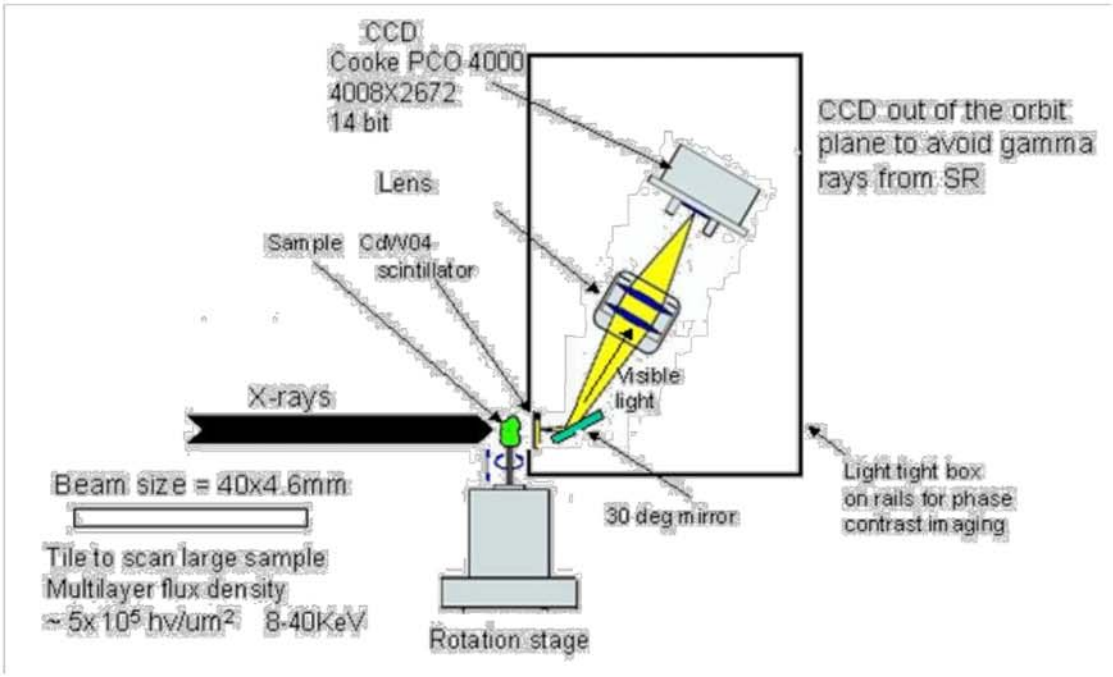


Figure 1.9 Schematic of the end station of the synchrotron x-ray tomography facility.

(Image from online source of beamline 8.3.2, ALS)

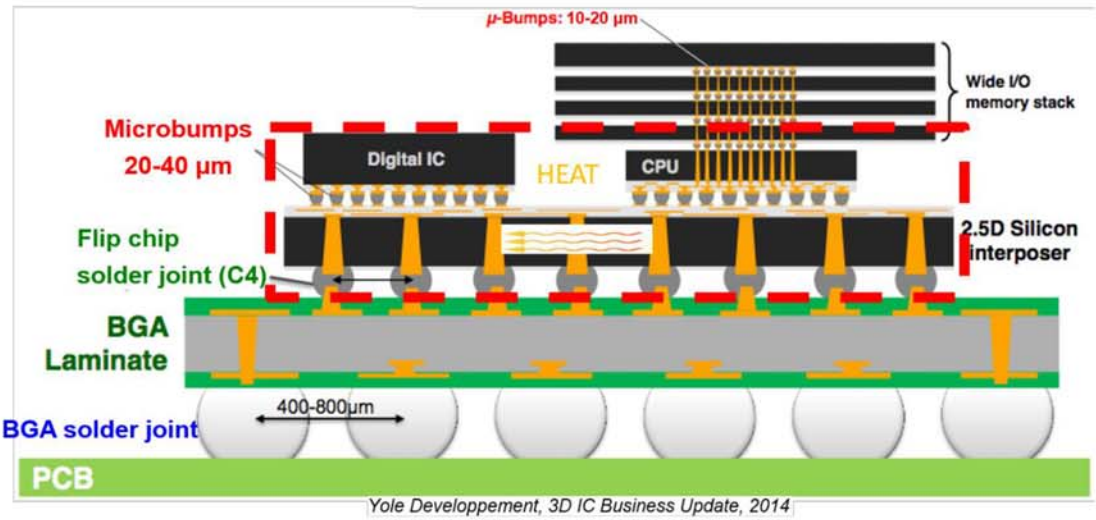


Figure 1.10 Schematic showing the horizontal heat transfer through Si interposer

(Adjusted image from ©Yole Developpment)

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Chapter 2 Joule Heating Enhanced Electromigration Weak Link

2.1 Introduction

With the trend of big data and internet of things (IoT), mobile device is becoming indispensable in daily life. Mobile technologies which enable broad applications with wider data bandwidth, faster response, lower power consumption, and smaller form factors are in demand. One of them pursued by the microelectronics industry is 3D stacking of several Si chips joined together by microbumps and TSVs. Homogeneous and heterogeneous integrations are possible for aggressive performance requirement [1-4]. At present, some simple 3D IC devices have already been introduced in mainframe computers for collecting field data of performance and reliability. However, the applications to mobile devices are behind schedule due to high cost and the effect of Joule heating on reliability. It is worth mentioning that high cost and Joule heating are of less concern in mainframe computers.

Because the reliability studies on 3D IC devices are not extensive yet, consequently we have little idea on its failure mode. The synergistic effects of Joule heating on electrical, thermal, and mechanical failures are not well known. In this chapter, we begin with the experimental procedure of system-level electromigration (EM) test to find out the weak link, and then discuss the physical analysis of the failure results.

2.2 Experimental Procedures

In this study, test samples are provided by Qualcomm. Fig. 2.1(a) and 2.1(b) show respectively an SEM cross-sectional image and an x-ray tomography image of our test sample. From the bottom, an array of very large ball-grid-array (BGA) solder balls of 250 μm is shown. Above the BGA is a polymer-based printed circuit board (PCB) containing plated-through-holes (PTHs) or substrate vias which were filled with thick Cu. On top of the board is an array of flip chip solder joints of 100 μm in diameter. Flip chip solder joints, typically are called C-4 (controlled-collapse-chip-connection) solder joints, connect the board and a Si interposer chip containing TSVs. On the interposer chip is an array of microbumps with diameters about 20 μm. Finally, a Si device chip is on top of the microbumps. In the above 3D structure, we must mention that there is a first set of RDL in the PCB, and the RDL is required in order to fan-out circuits from the BGA to the C-4 joints. Then, in the interposer, there is a second set of RDL in the interposer chip for the circuit transition from C-4 joints to microbumps. This second set of RDL is new in 3D IC because it is not required in 2D IC. We will show that this RDL is the weak-link in EM tests.

In Fig. 1(b), a set of arrows in blue color was used to indicate that we can pass electric current to study EM in the packaging circuit. We use one of the BGA balls on the left as the cathode and direct electrons to flow through the PTH, flip chip solder joint, TSV, and a daisy chain of microbumps, and then return in opposite direction to another BGA ball on the right as the anode. Since our EM test is only for a packaging circuit, we do not include transistors or multi-level Cu damascene

interconnects on the Si chip. Nevertheless, in the packaging circuit, we do have a large number of Cu connections in the TSV and RDL as well as solder joints. This system level EM test is much more complicated than those previous studies of EM in a pair of solder joints or a stripe of Cu or Al lines [5-8].

Before EM test, I-V curve of test samples were measured. Then we connected samples to power supply and did EM test. The EM testing conditions and life times of each test are listed in Table 2.1. The samples failed in a second when 100 mA passed through a pair of the BGA at 100 ℃. Based on this finding, three testing conditions of lower current were chosen at 100 ℃, 50 mA; 100 ℃, 60 mA; and 150 ℃, 50 mA.

To locate the failure site, those failed samples were polished layer by layer slowly and carefully with SiC papers down to 2500 grit and optical microscope was used to observe the cross-section in time to find the failure site. Then the cross-section was polished progressively with 0.1 and 0.05 μm Al_2O_3 powders and scanning electron microscopy (SEM) was used to obtain the image of the failure site. To obtain a better image of the failure site, focus ion beam (FIB) was used to cut perpendicular in to the failure site so that we can obtain very clear SEM image of the site.

2.3 EM Weak Link at the RDL in the 3D IC Package System

Fig. 2.2 shows the I-V curve by measuring the samples before EM test. We can see a straight I-V curve indicating that the samples indeed have a current path and ohmic behavior. The resistance change curves for some of the tests are shown in Fig.

2.3. Although under different testing conditions, some samples fail really fast, and some fail much slower, all of those failures show a rather flat resistance change with time until a sudden increase leading to failure. Just before the failure, a tiny increase of resistance about less than 5% can be barely observed. Because the period of recording data is 1 minute and 40 second, the abrupt increase in resistance meaning that within the period of failure, a dramatic damage occurs in the testing sample. Fig. 2.4(a) and 2.4(b) show the failure site images of the sample failed in 164 h at 100 ℃ and 50 mA; and Fig. 2.4(c) and 2.4(d) show the sample failed in 12.25 h at 150 ℃ and 50 mA. They were found in the RDL in the interposer chip. In Fig. 2.4(a), we can see six periodic holes in the RDL. Fig. 2.4(b) shows a clear image by using FIB to cut perpendicular into the failure site. These holes indicate a burn-out type failure, where we see that the Cu lines were molten and the dielectric materials were broken. Fig. 2.4(c) shows another failure site. This failure site is really big, about 80 μm long. FIB was used to cut three holes at the beginning, the middle, and the end of the failure site respectively to obtain more clear images. Those images are similar and one of them is shown in Fig. 2.4(d). All of them show the burn-out type failure.

2.4 Physical Analysis of the Failure Mode

Fig. 2.5(a) shows the location of RDL (weak link) in the sample. It is near the bottom side of the interposer and below the TSV. This RDL is served as the current fan out path when current passing from C4 solder joints into TSVs. Fig. 2.5(b) is a higher magnification image of RDL and the net structure of RDL can be seen. This net structure is made similar to Cu damascene structure but carries much higher current, as discussed below.

Fig. 2.6 is a cross-sectional TEM image of the Cu lines in RDL. The cross-section of the Cu line is about 100 nm by 100 nm. According to Fig. 2.6, if we assume 1 mA passes across the cross sectional area, the current density will be 1 x 10^7 A/cm^2, which is very high for EM to happen in Cu line at 100 ℃. The estimate of current density is not unreasonable. Because from the density change (number of joints per unit area) of BGA to C-4 solder joints and to microbumps, we expect it when the applied current is 50 to 60 mA.

Furthermore, the density of Cu line is extremely high in RDL, as the net structure shown in Fig. 2.5(b), which means that Joule heating is very serious. Also the heat dissipation is poor, so the temperature can have a time-dependent increase. Physically, we note that the thickness of interposer chip is about 50 μm as shown in Fig. 2.1(a), which is much less than the typical thickness of Si wafer at 200 μm. The heat conduction of Si interposer is much reduced and this is one of the reasons why heat dissipation is poor. These situations are very different from previous EM studies carried out in Cu and Al lines reported in the literature [9-13]. These special situations result in the new failure mode, the time-dependent failure of burn-out in EM test. In this failure, the temperature must be raised above the melting point of Cu, which is 1083 ℃. Below, we confirm the time-dependent Joule heating and the positive feed-back to EM by simulation.

A three-dimensional simulation program was adopted to show the possibility of burn out in the RDL wires at the stressing condition.. Fig. 7 shows the geometry of the modeled RDL unit. Here, the Cu wires have the dimension of 100 nm x 100 nm x

1.7 um, while the Cu via has the diameter of 100 nm, and height of 100 nm. Suppose there are 10 units to redistribute the current of 50 mA, each RDL unit will carry 5 mA. The current flow direction is from bottom (substrate side) to top (chip side). The generated Joule heating will be absorbed and conducted through the Cu wires and vias in the RDL structure. The physics of heat production and heat conduction in the Cu RDL structure is fully coupled, and governed by the following equation,

$$\rho C_p \boldsymbol{u} \cdot \nabla T = \nabla \cdot (k \nabla T) + Q \qquad \text{---(2.1)}$$

where ρ is the density of copper, C_p is the heat capacitance, k is the thermal conductivity, and Q is the power density induced by Joule heating. At the steady state, the RDL dissipates the generated Joule heating in two ways: from its upper side through silicon to the surrounding air (at 373K), and from its lower side through the substrate to the surrounding air. The dissipating process of heat fluxes to the surroundings is modeled using heat transfer coefficient, h. The inward heat flux is governed by the following equation:

$$q_0 = h \cdot (T_{ext} - T) \qquad \text{---(2.2)}$$

where q_0 is the inward heat flux, h is the thermal transfer coefficient (W/(m^2·K)), T_{ext} is the surrounding temperature. For the chip side, h is set to 90000 W/(m^2·K). For the substrate side, we set h to be 500 W/(m^2·K). These parameters are reasonable because the thermal conductivity of silicon is two orders of magnitude higher than the substrate. Since the Cu line in RDL is made similar to Cu damascene structure, we assume that the EM damage is also similar to Cu damascene structure by surface

diffusion at 100 ℃ in which a bi-model failure was found [9,14-15]. The first mode of failure is at the capping liner interface and the second is at the bottom of vias. Void formation at the capping liner interface will make Cu lines thinner in the current flow direction, while the void at the vias bottom will lead to opening. Because of the reduced cross sectional area of current path in Cu line, resistance and joule heating will increase. Due to poor thermal dissipation, the increased Joule heating will result in the increase in temperature, which in turn will increase the rate of EM. However, the enhanced EM will in turn increase resistance and temperature again. This positive feed-back process accelerates the thinning of the Cu lines in RDL. Fig. 2.7 is the temperature distribution result at the condition of 50 mA,100 ℃ when the Cu line is getting thinner, and we can see from Fig 2.7(d) that the joule heating of the Cu line could reach the melting point when EM depletes more materials. Fig. 2.8 is the simulation results in three different stressing conditions, from which we can see the synergistic and positive feed-back process leading to fast and catastrophic type of burn-out failure.

2.5 Summary

This synergistic effect of Joule heating and EM on burn-out is a new failure mode of reliability. Joule heating will be the critical issue as the density of transistor gets higher while the form factor cannot change much in mobile units. This synergistic effect can couple with mechanical and other failure in the future. Clearly, it needs our attention and more understanding.

In summary, we studied the system level EM in 2.5D IC test structures. Time-dependent burn-out type of failure sites has been located in the RDL between the C-4 joints and micro-bumps. Simulation results support the finding that the positive feed-back between Joule heating and EM can lead to a local temperature increase reaching the melting point of Cu. It can occur in a fast and catastrophic burn-out type of failure in the RDL in our test samples. To minimize the system level failure, the design of robust RDL by making it wider and supplying more vias should be helpful. In next chapter, we will discuss the work of power delivery design by optimizing the RDL to ensure robust power delivery within electromigration restraint.

2.6 Acknowledgement

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Note: The materials of Chapter 2 was published to Journal of Applied Physics, 2015.

2.6 Figures

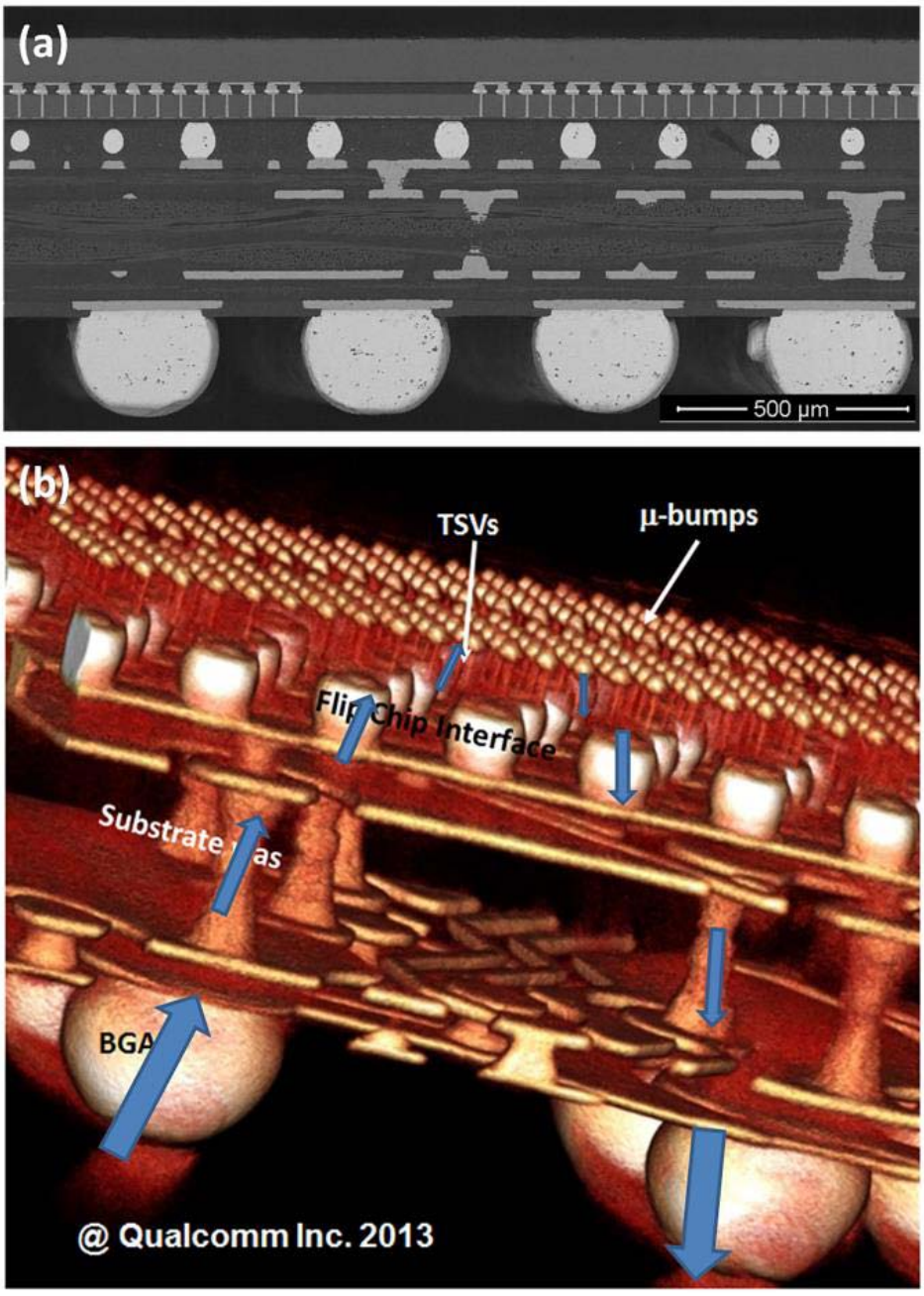

Figure 2.1 SEM cross-sectional image and an x-ray tomography image of our test sample.

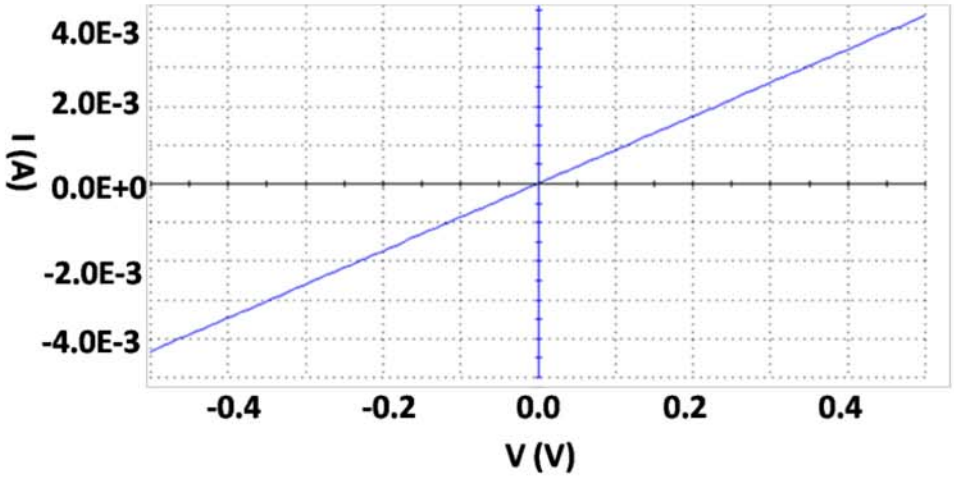

Figure 2.2 I-V curve of the current path in test sample

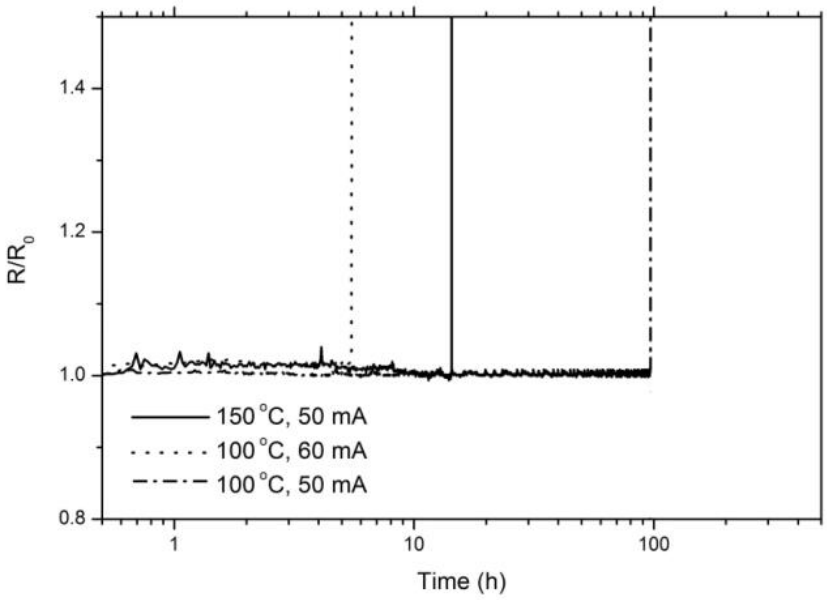

Figure 2.3 The resistance change curves for some of the EM test.

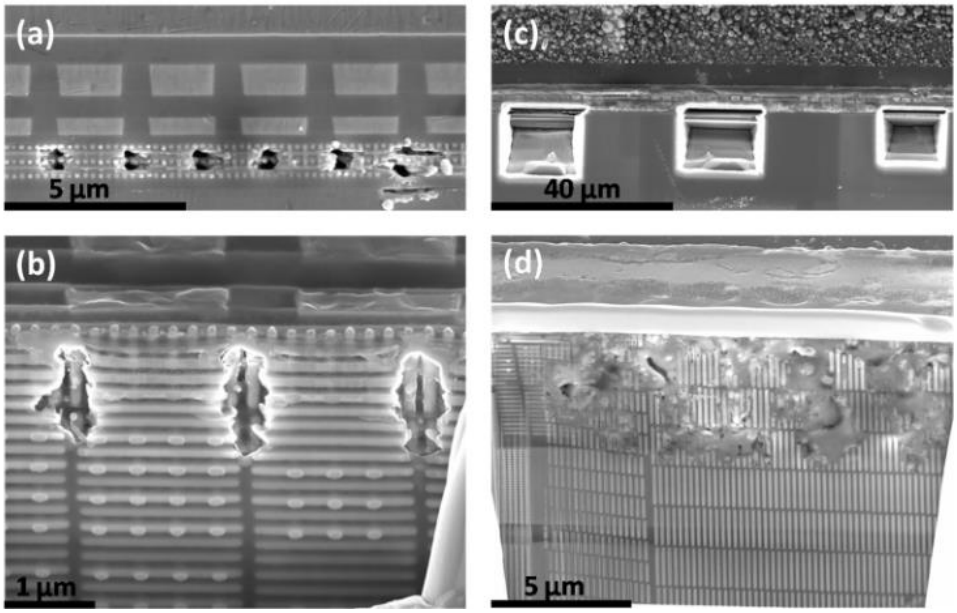

Figure 2.4 Failure site images (a) and (c) and their corresponding FIB cut images (b) and (d).

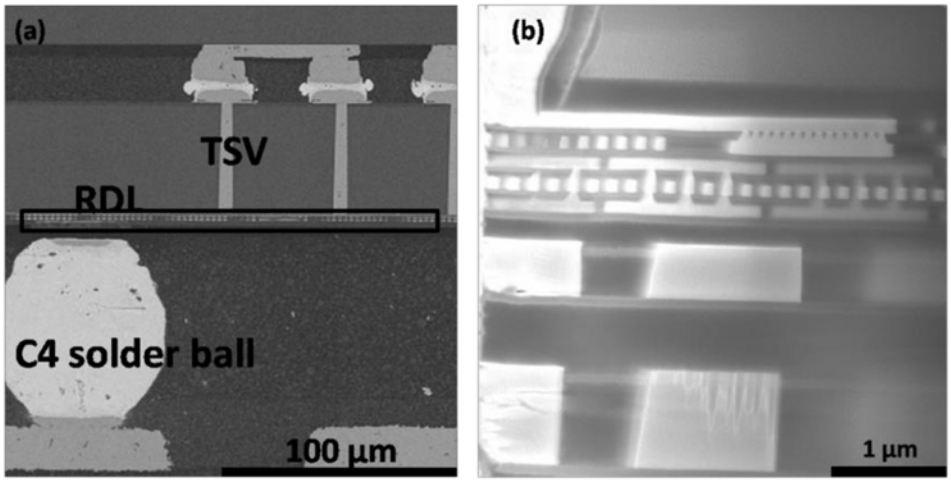

Figure 2.5 (a) Location of RDL and (b) SEM image of RDL.

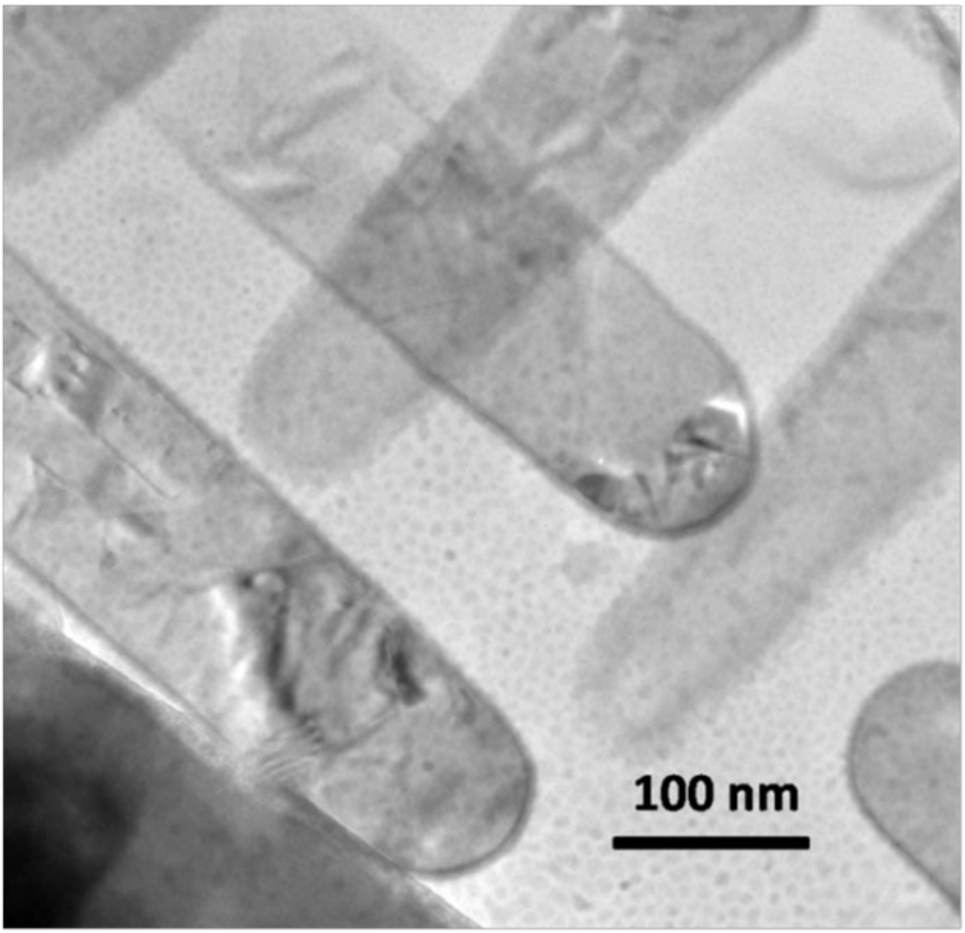

Figure 2.6 TEM image of Cu line in RDL.

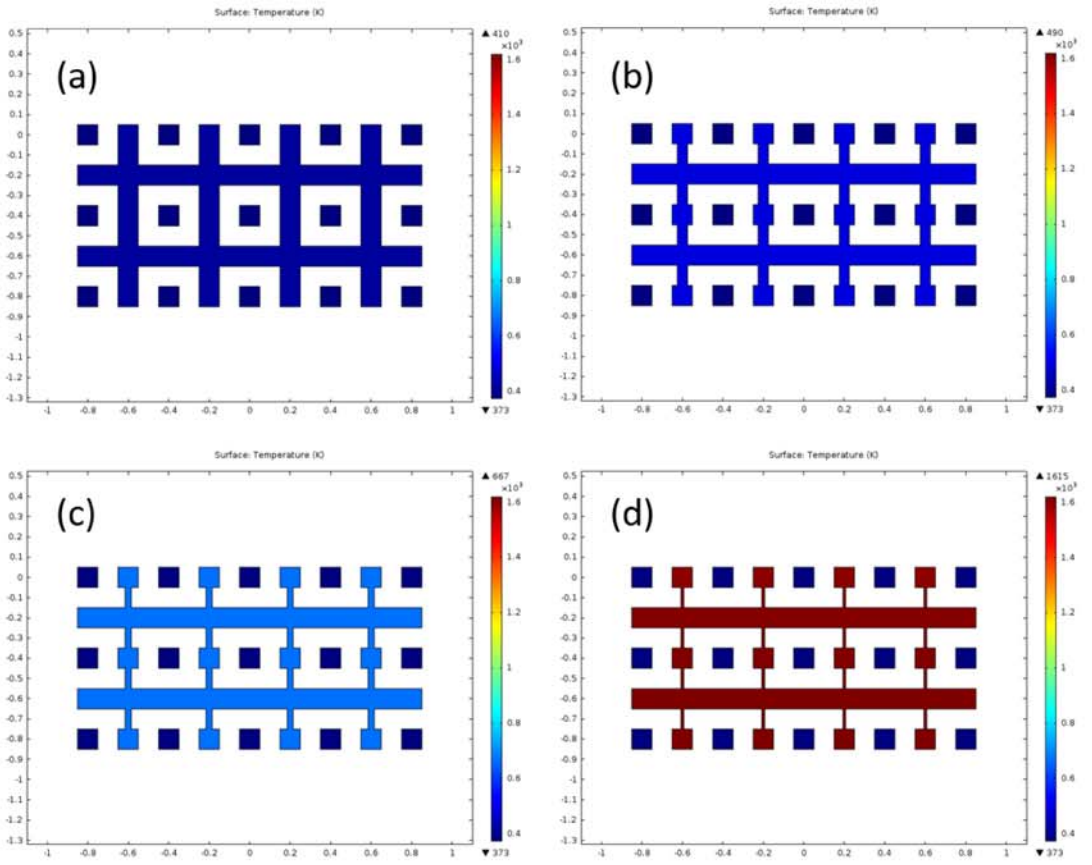

Figure 2.7 Temperature rise due to electromigration at test condition (50mA, 100°C)
(a) via diameter is 100nm; (b) via diameter is 50 nm;
(c) via diameter is 30 nm; (d) via diameter is 14 nm.

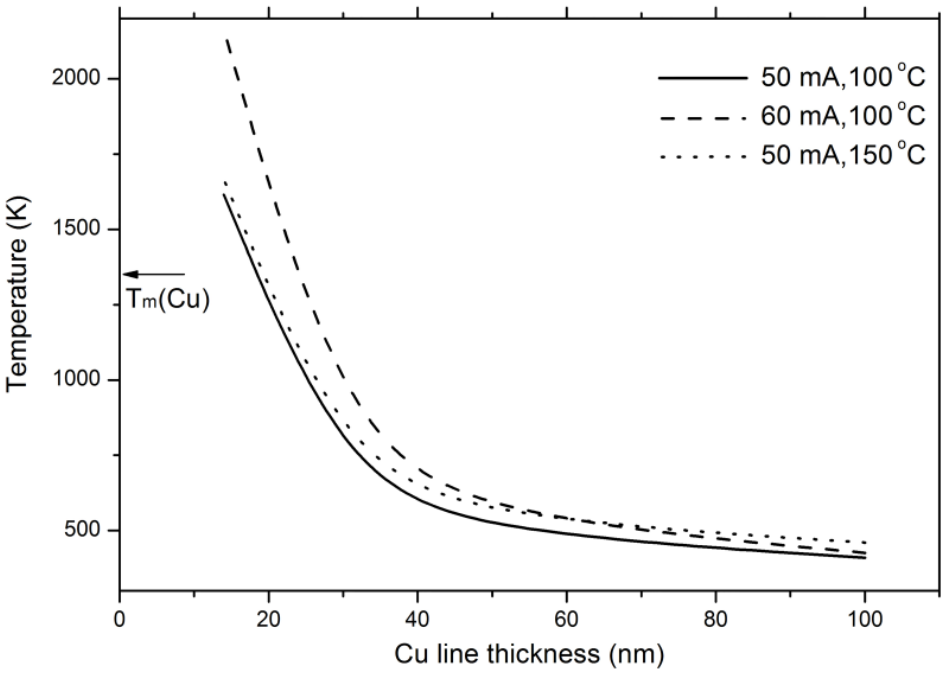

Fig. 2.8 Positive feedback between electromigration and joule heating at different test conditions.

TABLE 2.1. EM tests conditions and life times.

T (°C)	Current (mA)	Time-to-failure (h)		
100	50	164	384	461
100	60	5.5	6.25	30

150	50	12.25	14.3	148

2.7 References

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Chapter 3 Optimized Power Delivery for 3D Integration

3.1 Introduction

While the application of 3D integration memory products is now widespread [1-3], the extension to more challenging applications such as stacked processor on cache and more general logic stacking has lagged. There are two reasons for this and both relate to power delivery and design:

Logic chip stacks consume a lot more power (30-250W) so methods need to be developed to ensure uniform power delivery to both strata (we consider only two strata because of power considerations) and just as important we need efficient methods to extract the dissipated power. At 1 V, we need to deliver 30-250 A. Since the higher power strata must be proximate to the heat-sink, for example, in a processor-on-cache application, all power to that upper stratum must be delivered through TSVs in the bottom strata. This can seriously disrupt design efficiency. So it is incumbent on the design methodology to minimize the use of power and ground TSVs while simultaneously minimizing all IR drops (in the redistribution layers as well as in the TSVs) while maintaining a uniform grid.

Beside the IR drop, the electromigration is the reliability concern for power delivery. As we discussed in Chapter 2, the weak link for power delivery system is the redistribution layer (RDL). Therefore, the design for a robust power delivery system should optimize the design of RDL. However, previous design work [4-6] on 3D IC power delivery system usually assumed simple extension of TSV to the bumps without any redistribution layer, as shown in Fig. 3.1(a). The supply bumps are aligned with TSVs in every case. In addition, some other 3-D power delivery work has largely focused on the TSV cluster design [7] (also called TSV farms), which extends TSV bundle on one C4 bump, as shown in Fig. 3.1(b). While this works for relatively low power stacks, it is sub-optimal for high performance stacks. This design does not fully utilize the large current carrying capacity of TSVs. Furthermore, a high density TSVs in a small area, while less disruptive from a design perspective, may need further scrutiny from a thermo-mechanical stress perspective [8].

In this chapter, we address the problem of efficient power delivery to a high power stack. We assume a two-high stack due to power and thermal limitations and assume that the two strata are joined face to face. This is depicted in Fig. 3.2. This configuration allows for the largest number of connections between the two strata and the minimal use of TSVs.

We have designed in this paper a model package assembly for power delivery from C4 bumps to TSVs, and then to μ-bumps. In our design, we include two levels of redistribution layers, one is from C4 bumps to TSV – the "grind-side RDL", and another one is from TSV to μ-bump – the "fat-wire RDL". The μ -bump then delivers power to the upper strata via a conventional power distribution methodology. Also, we do not use one C4 to one TSV power delivery, instead we use multiple C4s connected to a single TSV, and then fan the TSV out on the top to multiple μ-bumps. The electrical and geometric parameters of Cu lines in RDL are based on the GLOBALFOUNDRIES 32 nm technology, and we connect the TSV to the second to last metal line, the so-called fat wire level, which is much thicker than the first level metal line. It is also possible to use a so-called super fat wire level, which is ~3X thicker. We will discuss this later. We also compared the two types of TSVs that are already manufactured. A cylindrical TSV refers to the common TSV where a cylindrical metal layer is surrounded by an insulation layer. In an annular TSV, there is a Si core surrounded by a metallic conductor and isolation materials. Compared to previous efforts, we demonstrate the benefits by evaluating the current density distribution and IR drop of each level. The annular TSV has a larger cross-sectional area and thus a lower resistance.

3.2 Design Methodology

In our work, we assume a cylindrical TSV has a diameter of 5 μm and height of 50 μm which is according to the industry TSV size, we assume the diameter of C4 bump is 100 μm. And we assume μ-bumps are 25μm in diameter. According to the electromigration behavior of each component, the current carrying capability of each component at an operating temperature (~ 100 ℃) is shown in Table 3.1. From the values, we note that one TSV (5 μm diameter) can carry about 4 times more current than C4 bump (100 μm in diameter), and 8 times more current than μ-bumps with 25μm in diameter. Therefore, in our design, we use one TSV to connect eight μ-bumps by using front-side fat wire level, and at the bottom the TSV will fan current out to four C4 bump by using grind-side RDL. And we assume the current source is 1A per unit cell. Fig. 3.3 shows one unit cell of our design.

3.3 Simulation Results of Optimized Design

To study the electrical performance of our design, models have been established using the finite element method. For the models in this section, we have used the parameters of TSVs and μ-bumps in [12]. The diameter of TSV is 5 μm, and the height is 50 μm, and the TSV conductor is Cu. We have neglected the barrier and seed layers assuming they carry negligible current. This is a valid approximation as Cu dominates the TSV. The diameter of μ-bumps is 25 μm, and the height is 35 μm. The material of μ-bumps is assumed to be Cu_6Sn_5 (complete IMC conversion). The material for the RDL is Cu, the thickness of fat wire RDL line is 1.2 μm, which corresponds to the second to last fat wire level thickness in the

GLOBALFOUNDRIES 32 nm technology. The material for C4 bumps is predominantly Sn, and the diameter is 100 μm. The materials properties are listed in Table 3.2.

3.3.1 Electrical Simulation Results for the Front Side

For the front-side analysis, we include μ-bumps, front-side fat wire RDL, and TSVs into consideration. Fig. 3.4 shows the design concept for the front-side fat wire RDL, and the circle in the square pad is the TSV. The current exits from TSV, and all the way up to the square pad, and then fans-out to eight terminal pads which will receive μ-bumps from the upper strata. In order to keep the IR drop from TSV to μ-bumps above each terminal to be the same, the electrical resistance from the TSV to each terminal pad must be identical. Since all the wiring is at the same level, and we assume identical wire widths the distances must be made identical. For example, if we compare terminal 5 and terminal 6, we need to have d1+d2=d0, assuming current is uniformly distributed without current crowding. However, if we consider current crowding when the conductor has sharp turns, the current will crowd near the sharp angle. For example, in Fig. 3.4 the current needs to follow turns in the conductor to reach the terminal 5, instead of going uniformly like the black arrow, the current will go through the red arrow, which travels shorter distance than the black arrow. Then, because of the shorter distance, most of the current will travel in this route, resulting in a higher current density for the μ-bumps above terminal 1, 3, 5 and 7. In order to estimate how big the current crowding effect is, we simulated this structure by populating μ-bumps in these positions, as shown in Fig. 3.5. We explain in details below.

Fig. 3.5(a) is the top view of the front side design, there are eight μ-bumps at the top, marked #1 through #8. The coordinates of the even μ-bumps are (0, ±70 μm) or (±70 μm, 0), and the coordinates of the odd μ-bumps are (±35 μm, ±35 μm). Therefore, the distance between each μ-bump to the center of the pad is the same. Instead of using a square pad, we use a cheesed pad with some holes inside, as shown in Fig. 6(b) and the holes are filled by dielectric. The use of cheesed pad is required for uniform chemical mechanical polishing (CMP). Also, instead of using a wider wire of 6 μm in width, we have used three wires of 2 μm in width, and the separation is also 2 μm. The thickness of the front-side fat wires is 1.2 μm. The use of three wires instead of one wider wire will help the current spread evenly in different wires even through there is a hole at the middle of the edge in the cheesed pad, as shown in the dashed red box in Fig. 3.5(b). The existence of the hole will cause the current to detour around the hole, and then fan-out to the Cu lines. We supply 1A current from the bottom of TSV, and the current goes up through the TSV to the cheesed pad, and then fans out to the eight μ-bumps. The current density of each fat wire RDL is the same, as shown in Fig. 3.5(c). When we add μ-bumps, the current density distribution of μ-bumps is shown in Fig. 3.5(d), from which we can see the current densities of the inner bumps are 1.25 times higher than the outer bumps due to current crowding effect. This 25% difference is unacceptably large suggesting that we need to consider current crowding in the design.

When we consider current crowding, we need to space the inner μ-bumps further away. For μ-bumps, we design the pitch (the distance from the center of one μ-bump to the center of its closest neighboring μ-bump) to be 50 μm. By setting the

coordinates for inner μ-bumps to be (±36.3 μm, ±36.3 μm), and that for the outer μ-bumps are (0,±70 μm), (± 70 μm,0), we are able to obtain the current density distribution of each μ-bump to be the same while keeping the pitch 50 μm.

The top view placement of μ-bumps with consideration of current crowding effect is shown in Fig. 3.6(a). When supplying 1A current, the current density distribution result of the μ-bumps is shown in Fig. 3.6(b), the IR drop of front-side fat wire level is shown in Fig. 3.6(c), and the IR drop of μ-bumps is shown in Fig. 3.6(d). From Fig.3.6, we can see that the average current density in the μ-bumps is 2.64×10^4 A/cm^2, and the IR drop of μ-bump is 0.002 V. The average current density of front-side fat wire level is 1.1×10^6 A/cm^2, and the IR drop of the front-side fat wire level is 0.023 V.

3.3.2 Electrical Simulation Results for the grind-side RDLs

For the grind-side design, the TSV, grind-side RDL, and C4 bumps must be taken into consideration. On the grind side, one TSV will fan out current to four C4 bumps. And the pitch between the C4 bumps is 150 μm with the diameter of C4 bumps to be 100 μm. The four C4 bumps are at the corner of square with TSV in the center. The thickness of the grind-side RDL is 3 μm. Fig. 3.7 shows the 3-D and top view of the grind-side design.

The pad at the grind side is not cheesed as it is fabricated using a build-up process. When supplying 1A current, the current density distribution and IR drop of each component at the grind-side is shown in Fig. 3.8. Fig.3.8 (a), (b), (c) show the

current density distribution of TSV, the C4 bumps and grind-side RDL. Fig.3.8 (d), (e), (f) show the IR drop of the three components. From Fig. 3.8, we can see that the average current density in the TSV is 5.0×10^6 A/cm^2, and the IR drop for TSV is 0.04V; the average current density of grind-side RDL is 1.1×10^5 A/cm^2, and the IR drop for the grind-side RDL is 0.01V; the average current density of C4 bumps is 4.0×10^3 A/cm^2, but we emphasize that the current density in the C4 bumps is not uniform, and the IR drop for the C4 bumps is 0.0007V. The maximum current density in the grind-side structure is at the interface between TSV and the top cheesed pad, which is 4.9×10^7 A/cm^2, one order higher than the average current density in TSV. This is because the hole in the middle of the cheesed pad reduces the contact area between cylindrical TSV and the cheesed pad. Therefore, we recommend not to cheese in the middle.

Table 3.3 is the summary of the IR drop of each component, and their contribution. From Table 3.3, we can see that in the case of cylindrical TSV with fat wire, the TSV and front side fat wire RDL are the main contributors for the IR drop. This is because the thickness of the fat wire we use is 1.2 μm, which is at least 10 times thicker than the thinnest metal line in the Cu multilayer interconnects. Therefore, the IR drop of the RDL decreases a lot, and is at the same order of IR drop of TSV. However, the total IR drop of 76 mV is still large and represents an IV power dissipation of 76 mW per cell, if each cell carries 1A. Then the total power grid dissipation for the chip that requires 30A would be 2.28 W and for a 300W chip it would be 22.8W an automatic reduction in efficiency of 7.6%. This is not negligible. We now address how to improve this below.

3.4 Discussion of Further Improved Power Delivery Design

3.4.1 Annular TSV vs. Cylindrical TSV

Besides cylindrical TSVs, annular TSVs are also used in the industry [13]. An annular TSV (Fig. 3.9), consists of a silicon-filled core surrounding by a metallic (usually Cu) annulus. We use the parameters of the annular TSV in GLOBALFOUNDRIES to compare. The diameter of the inner core is 8 μm, while the diameter of the outer ring is 19 μm. After running simulation, we found that the IR drop of annular TSV is 0.004V, which is one order smaller than the solid cylindrical TSV. The reason is that the annular TSV has larger cross-sectional area, but it also occupies larger space compared to cylindrical TSV. We show below that the larger TSV size is a sensible tradeoff. As the fraction of area occupied by cylindrical TSVs for power delivery is only 0.2 % of the die area considering the maximum Keep-Out-Zone (KOZ). Using annular TSVs reduces the dissipated power in the power delivery circuits by 48% while increasing TSV occupation area (TSV+KOZ) by only 0.37%.

3.4.2 Fat Wire RDL vs. Super-fat Wire RDL

Even if we use fat wires with thickness of 1.2 μm at the front side, the IR drop of RDL is still the main contributor. By changing the processing from dual damascene to single damascene process, it is possible to fabricate super-fat wire with thickness to be around 3.5 μm. If we use super-fat wire, the IR drop will be even less, and reduced by 70% compared with fat wire, as shown in Table 3.3 – a further reduction in dissipation of another 22% for the total system.

So the use of annular TSVs and super fat wires represents a power savings of almost 70% in power supply grid dissipation, bringing dissipated power supply power from 22.8 W down to ~7 W for a 300W die.

3.4.3 Power Delivery Network

We now present details on the full power delivery network. By using the unit design above, we generated the power delivery network; the lattice is shown in Fig. 3.10. Vdd is the power line while Vgnd is the ground line. The circuit is between Vdd and Vgnd (not shown). The spacing between each Vgnd is 600 μm. If we don't consider the KOZ of TSV, then the cylindrical TSV will occupy 0.009% of the Si. Usually, the minimum KOZ is 2 μm while the maximum KOZ is 10 μm. If we consider KOZ to be 2 μm, then the cylindrical TSV will occupy 0.03% area of Si die. If we consider the KOZ to be 10 μm, then the cylindrical TSV will occupy 0.2%. This means even we use the maximum KOZ to design cylindrical TSV, we still occupy less than 1% area of Si, which is acceptable. In case we use the preferred annular TSV and don't consider KOZ, using the above design lattice, the annular TSV will occupy 0.13% area of Si die. If we consider minimum KOZ to be 2 μm, the annular TSV will occupy 0.20%. If we consider maximum KOZ to be 10 μm, the annular TSV will occupy 0.57%. This means when we use annular TSV, although it will occupy marginally more space than cylindrical, it is much superior for power delivery and also reduces power dissipation.

3.4.4 Thermal Analysis

When we apply current to the unit, the resistive heating is Joule heating. By using the same technique in Chapter 2.4, and assume the thermal transfer coefficient h of the chip side (above micro-bumps) to 50000 W/(m2·K) while substrate (below C4 bumps) side h to be 500 W/(m2·K), we simulate the unit cell with both the cylindrical TSV and annular TSV for the temperature distribution after applying 1A current. Fig. 3.11 shows the temperature distribution of the unit cell in three different cases. With the assumed values of thermal transfer coefficient, the Joule heating will increase the device temperature to 322K for cylindrical TSV and fat wire level (Fig. 3.11(a)). Since the ambient temperature is assumed to be 293.15. This means the temperature increase is 28.85K in this case. And the temperature is highest around TSV, especially the interface between TSV and front-side RDL. By replacing cylindrical TSV with annular TSV, the temperature increase will be decreased to 9.85 K (Fig. 3.11(b)), much smaller than cylindrical TSV. If we use the annular TSV with super fat wire level, the temperature increase is further reduced to 6.85K. From the thermal analysis, we can see that the replacement of cylindrical TSV to annular TSV is critical to reduce the Joule heating.

3.5 Experimental Evaluation of EM Resistance of the Fat Wire RDL

3.5.1 Introduction of Test Vehicle

In this study, test samples are provided by GlobalFoundries. The test structure is dedicated to make the average current density at TSV, and TSV/RDL interface higher. Fig. 3.12 shows the TSV processing procedures. This TSV is fabricated by TSV-last

technique. The Back End of Line (BEoL) and transistors are fabricated first, and then blind hole was etched and electroplated with Cu, followed by capture RDL (device side) electroplating, as shown in Fig.3.12 (a). Then, the wafer was attached to a glass handler and thinned until close to TSV, shown in Fig.3.12 (b) and (c). The Si is then etched selectively by Reactive Ion Etching (RIE) to expose TSV out, shown in Fig.3.12 (d). Then the grind-side RDL is electroplated, and attached to a glass handler, shown in Fig.3.12 (e) and (f). And the glass handler at the capture side is removed.

The EM test structure is shown in Fig.3.13 (a) to (d). Fig.3.13 (a) is the schematic of the top view of the layout. In this schematic, the capture level RDL (1.2 μm thick) is shown in purple. We can see there are wires in the capture level to ensure robust power delivery. The grind-side RDL is shown in light blue, which is 25 μm wide, and 3 μm thick. The solid TSV (6.4 μm in diameter, 55 μm in height) is shown in red circle, and connected through grind-side RDL. The current is delivered through F+ and F- pad, and the voltage is measured through S+ and S- pad during EM test. Fig.3.13 (b) shows the magnified image of the cheesed pad above TSV. The pattern of this cheesed pad is designed to facilitate Chemical Mechanical Polishing (CMP) process. Meanwhile, the cheesed pad connecting TSV also have hundreds of small vias at the top, which are used to connect to the last metal wire level. Fig3.13 (c) is 3-D image of the circuit by Synchrotron radiation (SR) microtomography, from which we can also see there are two levels of wiring system in the capture side. Fig.3.13 (d) is the schematic showing the two wiring system connected through hundreds of vias. It is noted that wherever there is a cheesed pad, there are small vias connect in between.

Because TSV has a small diameter (~5 μm), but larger height(~ 50 μm), the traditional way (SEM or FIB) to characterize TSV is hard to perform. For example, a small tilt during polishing will make TSV appear at the top but disappear at the bottom, which makes it hard for SEM sample preparation. If we use Focued Ion Beam (FIB) to do failure analysis, it is quite time-consuming to cut a cross-section of 50 μm in deep, which means FIB is not useful for failure analysis with large amount of samples. Meanwhile, both SEM and FIB are destructive 2-D technique. Therefore, the need for high-resolution and non-destructive technique to do failure analysis quantitatively in three-dimensional is critical for TSV analysis. In this paper, we will demonstrate Synchrotron radiation (SR) microtomography technique to analyze the void and hillock formation at TSVs stressed by electromigration test. The 3-D imaging experiments were conducted on the microtomography Beamline 8.3.2 at the Advanced Light Source of Lawrence Berkeley National Laboratory. The general technique has been described before [14]. The special resolution of Synchrotron radiation (SR) microtomography in this experiment is 0.633 μm.

3.5.2 Experimental Procedures

Before EM test, we scanned the sample in the as received state by microtomography to show the circuits and microstructures. For this structure, electron flow is from the top capture level wiring to one of the TSVs to the grind-side RDL wiring and then to another, as illustrated in Fig. 3.14 (a). The microstructures of different components in the as-received state are shown in Fig. 3.14 (b) to (e). From Fig. 3.14 (b), we can see that TSVs have necking at the top part where etching recipe is changed from etching Si to etching SiO_2. Fig. 3.14 (c) shows the capture level, from

which we can clearly see seven wires are fanned out from the cheesed pad. Fig. 3.14 (d) shows the grind side fat wire, from which we can see that there is a dimple in the grind side RDL area connecting to the TSV. This dimple was possibly due to the over-etching in the fabrication process. Fig. 3.14 (e) shows the cross-section of the testing structure, from which we can see a pair of TSV is connected through the grind-side RDL.

Before EM test, I-V curve of test samples were measured. Then we used wire bonding technique to connect the power pad (F+, F-) and sensing pads (S+,S-) to the external pins. The wires are Al wires with 38.1 μm in diameter. Then we connected power pins (F+, F-) to power supply and connected sensing pins (S+, S-) to multimeter. The optical image of wire bonded structure is shown in Fig. 3.15 (a). The DC current is pumped through power supply and the voltage between S+ and S- is recorded during the EM test. The EM testing conditions and life times of each test are listed in Table 3.4. The failure time in this table is based on 10% resistance increase. The stressing current is 150mA, 200mA, and 300mA, which corresponds to the current density of 4.7×10^5 A/cm^2, 6.2×10^5 A/cm^2, and 9.3×10^5 A/cm^2. Fig. 3.15 (b) shows the optical image of one sample after complete open (testing condition is 200mA, and 300℃). The Al wires were removed in Fig. 3.15(b), and we can see that the cathode side was burned out. This was due to the EM induced void at the cathode side which has significantly increased the resistance, and hence the local Joule heating at the cathode. Therefore, some part of the cathode side is melted after failure.

3.5.3 Experimental Results and Discussion

Fig. 3.16 shows the I-V curve by measuring the samples before EM test at room temperature. We can see a straight I-V curve indicating that the samples indeed have a current path and ohmic behavior. The resistance of the testing structure is 0.013 Ω. The resistance change curve during the EM test is shown in Fig. 3.17. We evaluated the failed sample by X-ray microtomography to show the 3D view of the failure site, as shown in Fig. 3.18. Fig. 3.18 (a) shows 3D structure from the grind-side. We included two structures in Fig. 3.18 (a). The left structure is the untested structure for reference, which has the same thermal history. The structure at the right hand side is the testing structure. We can see that there is no obvious degradation in the reference structure, but there is depletion of the cathode TSV, depletion of the cathode TSV/RDL interface, and extrusion of the anode TSV/ grind side interface observed in the failed structure, which are more clearly shown in Fig. 3.18 (b) and Fig. 3.18 (c). Due to the possibility of melting, the void at the cathode might be larger than the EM induced void, therefore we use the hillock formation at the anode side TSV to do quantitative analysis. The atomic flux at the anode side due to Huntington model[15] can be expressed in the following equation:

$$J_{EM}^{total} = -CD_s\Omega\frac{\frac{d\sigma}{dx}}{kT} + CD_s\frac{Z^*eE}{kT} \quad \text{--- (3.1)}$$

where J_{EM}^{total} is the total atomic flux induced by EM, C (=1/Ω, Ω is the atomic volume of Cu) is the concentration of atoms per unit volume of the Cu, Ds is the effective surface diffusivity of the Cu at 300 ℃, Z* is the effective charge number, dσ/dx is the backstress gradient along the electron flow path, E is the electric field, where E = ρj, and ρ is the resistivity of Cu at 300C (3.51×10^{-8} Ω·m), and j is the applied current density in TSV (6.21×10^{5} A/cm^2), and k and T are Boltzmann's constant and

temperature, respectively. By assuming all the stress are released and the back stress gradient is zero, the equation above can be simplified as:

$$J_{EM}^{total} = CD_s \frac{Z^* eE}{kT} \quad \text{--- (3.2)}$$

And

$$D_s Z^* = J_{EM}^{total} \cdot C \frac{eE}{kT} \quad \text{--- (3.3)}$$

The J_{EM}^{total} is the total number of atoms per unit time per unit area. In obtaining the J_{EM}^{total}, an intensity-based segmentation algorithm by Avizo™ was used to label the extrusion at the anode and thus, by counting the number of voxels labeled as extrusion, the volumes and cross-sections of the voids can be determined, where the error was within ±10%. Fig. 3.19 shows the labeled extrusion in yellow color. In this case, the voxel count is 2097, and each voxel is 0.633×0.633×0.633 μm^3, while 0.633 μm is the scanning resolution. Therefore, the extrusion volume is 531.87 μm^3. The atomic volume (Ω) of Cu atom at room temperature is $1.182\times10^{-29} m^3$, which equals to 1.182×10^{-11} μm^3, and the powering time is 327744.89 sec. The effective area is 32.17 ($\pi\times3.2^2$) μm^2, thus

$$J_{EM}^{Total} = \frac{V}{\Omega At} = \frac{531.87}{1.182\times10^{-11}\times32.17\times329744.89} = 4.24 \times 10^6\ atoms \cdot um^{-2} \cdot s^{-1} \quad \text{--- (3.4)}$$

And then we plugged the J_{EM}^{Total} into equation (3.3), we can get the product of D_s and Z* to be$1.137 \times 10^{-10} \frac{cm^2}{s}$. On the other hand, if the back stress gradient is taking into account, the Ds Z* value would be higher.

A three-dimensional simulation program was adopted to show the current density distribution at the stressing condition. The simulation results are shown in Fig. 3.20. We can see that the TSV is subjected to higher current density than both RDLs, and the maximal current crowding occurred at the TSV/capture RDL interface which is twice the value of the TSV/ grind-side RDL interface. Both interfaces have high current density gradient due to the current crowding effect. However, the experimental results showed that TSV/grind-side interface is the flux divergence interface that has atomic accumulation even though the current density here is lower than the RDL/capture level interface. Here, we present the possible reasons: First, due to manufacturing, the TSV diameter at the capture level interface is widened by about 10%, while there is a dimple at the TSV/grind side RDL which might cause a thickness decrease by about 10%. This geometry difference will cause a lower current density at the capture level interface and increased current density at the grind-side interface. Second, the capture level has two wiring system, and the capture level interface is fully protected by diffusion barrier at both TSV side and local via side. However, the grind-side RDL is only protected at the TSV side. Therefore, the surface protection of the grind-side RDL is weaker, especially the interface of grind side RDL and glass handler. This interface might act as free surface for electromigration of Cu, which will cause mass depletion and atom accumulation at this surface. The schematic is shown in Fig. 3.21. We also observed rough surface of grind side RDL in the untested structure by X-ray tomography, as shown in Fig. 3.22, which serves as an experimental proof the surface weakness of grind side RDL.

3.6 Summary

In this chapter, we have proposed an optimal power delivery scheme unit based on the current carrying capability of each interconnect in 3D IC in order to minimize the use of TSVs, which cause design disruption. We studied the current density distribution and IR drop of our design based on finite element modeling. There is current crowding at the interface, and near corners. By considering the current crowding effect, we modified the μ-bumps placement to evenly distribute current to each μ-bump. The electrical simulation results show that TSV/fat wire interface has highest current density. Also the cylindrical TSV contributes to highest IR drop if we use fat Cu (1.2 μm) wire for RDL. We also compared cylindrical TSVs with annular TSVs. The results show that annular TSV can reduce the IR drop by one order of magnitude. Although annular TSVs occupy more area on Si chip, the TSV area is typically <1% even we consider maximum KOZ around TSV. In addition, we compare the use of super-fat wires instead of fat wires, the IR drop will decrease by 70%. The thermal simulation results suggest that the Joule heating induced temperature increase in the annular TSV is only 1/3 of the cylindrical TSV case. Therefore, the use of annular TSV, super-fat front-side RDL, and grind-side RDL are recommended for power delivery based on IR drop concern and Joule heating concern. We further evaluated the power robustness of the fat wire RDL and cylindrical TSV by 3-D SR X ray micro-tomography. The results shows better power delivery resistance to electromigration compared with the RDL design in Chapter 2. The products of effective diffusivity and the effective charge number, DZ* of TSV was measured at 300 ℃. The flux divergence place was found to be at the grind-side RDL/TSV interface. Simulation results indicate this interface has higher current density gradient but not the maximal current density. We further discussed the

possibility of less protection by diffusion barrier at the grind side that makes grind-side RDL weaker for electromigration than capture level RDL.

Note: In this chapter, the materials from section 3.1 to section 3.5 was presented at 2016 ECTC.

3.7 Figures

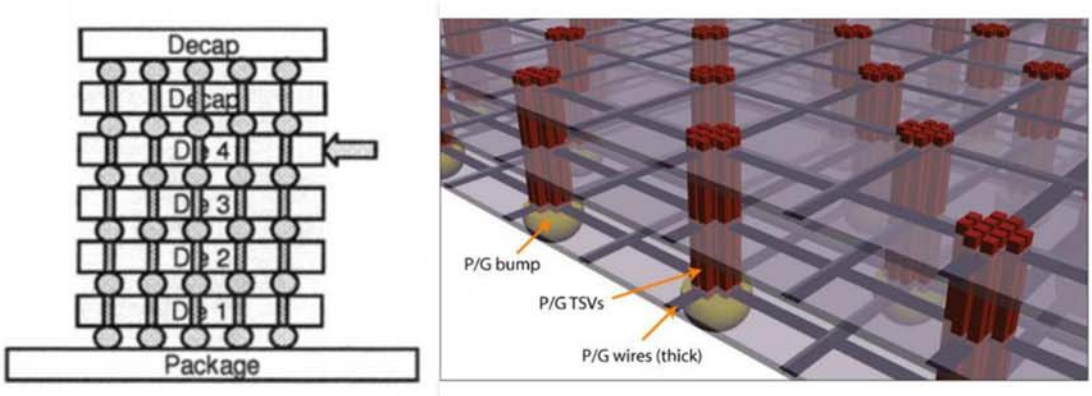

Fig. 3.1 (a) Schematic of simple extension of TSV to bumps [4] ; (b) TVS cluster [7] (reproduced with permission).

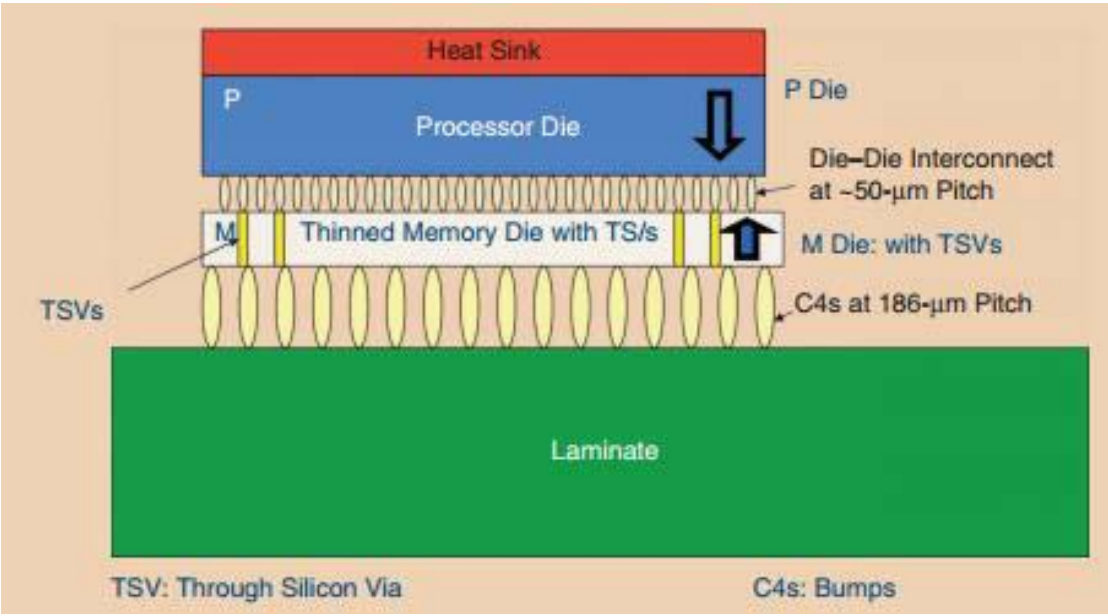

Fig. 3.2 A packaged two-high 3-D stack in the Face–Face embodiment.

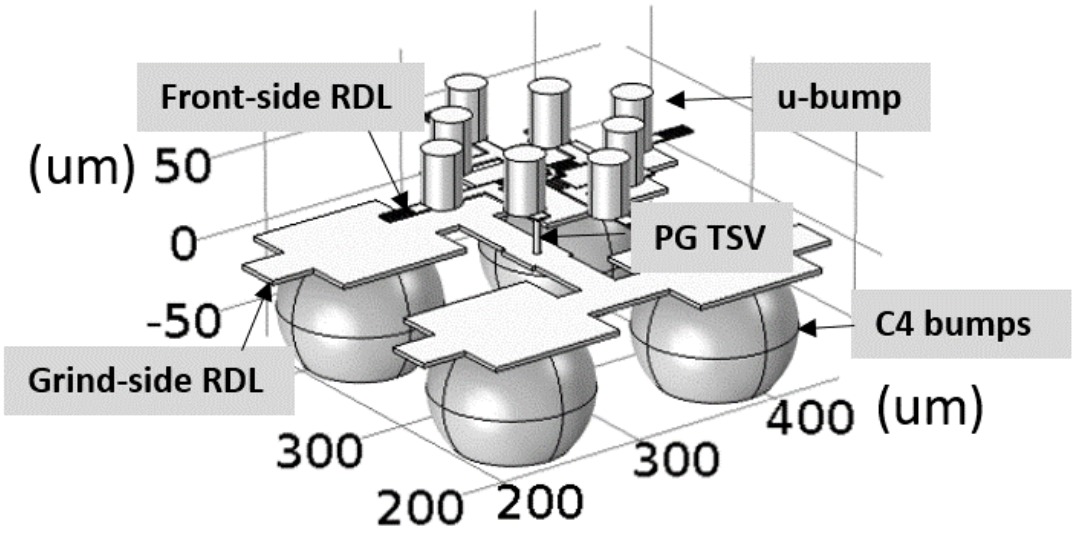

Fig. 3.3 3D IC power delivery system unit-cell model.

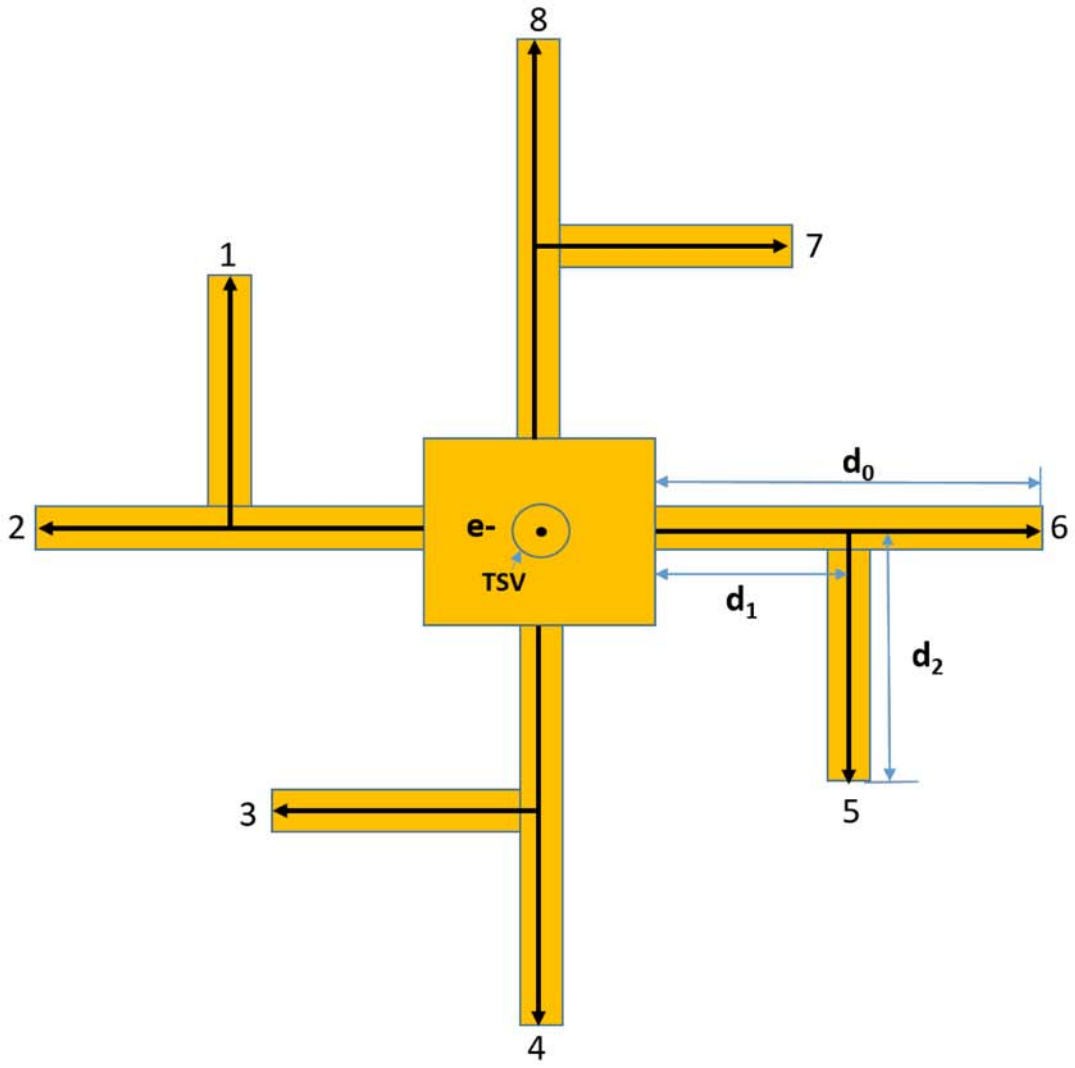

Fig. 3.4 Design idea of front-side fat wire level.

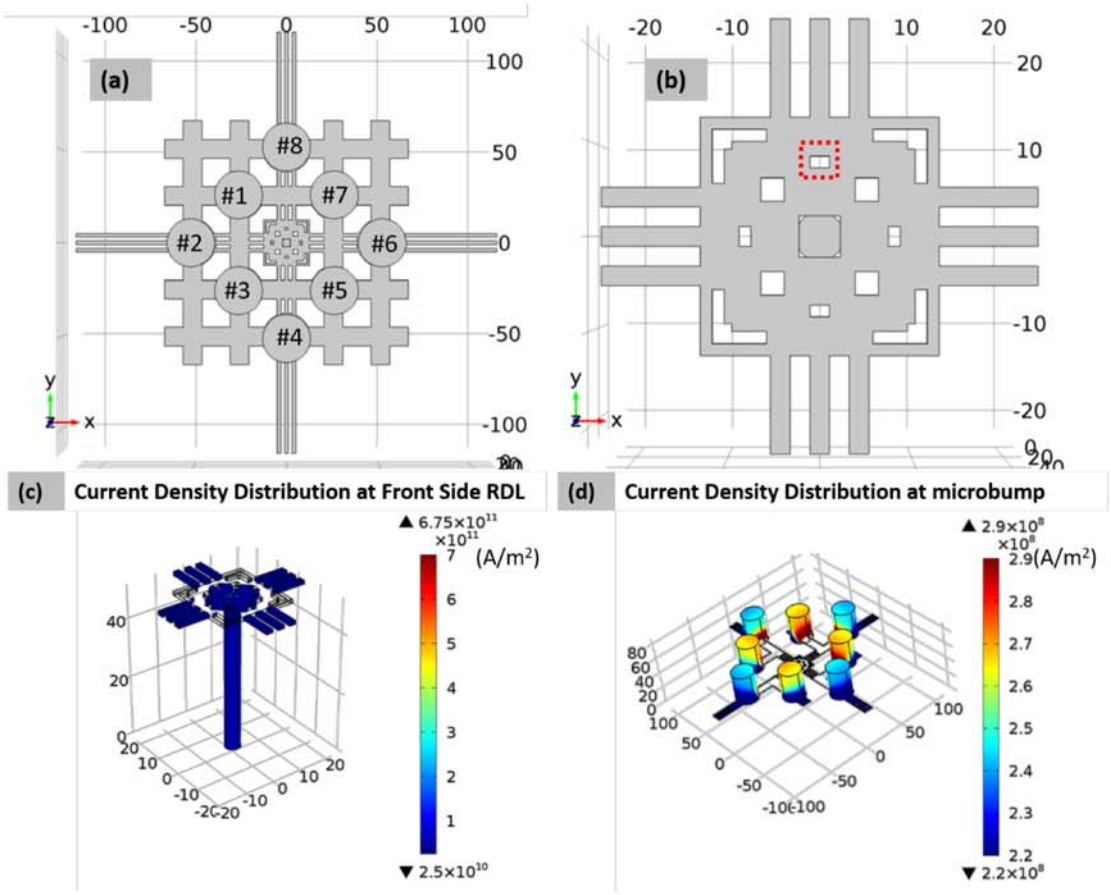

Fig. 3.5 Front-side design and current density distribution by neglecting current crowding effect (a)Top view of front side design; (b) Cheesed pad and RDL;(c) Current density distribution of RDL; (d) Current density distribution of μ-bumps.

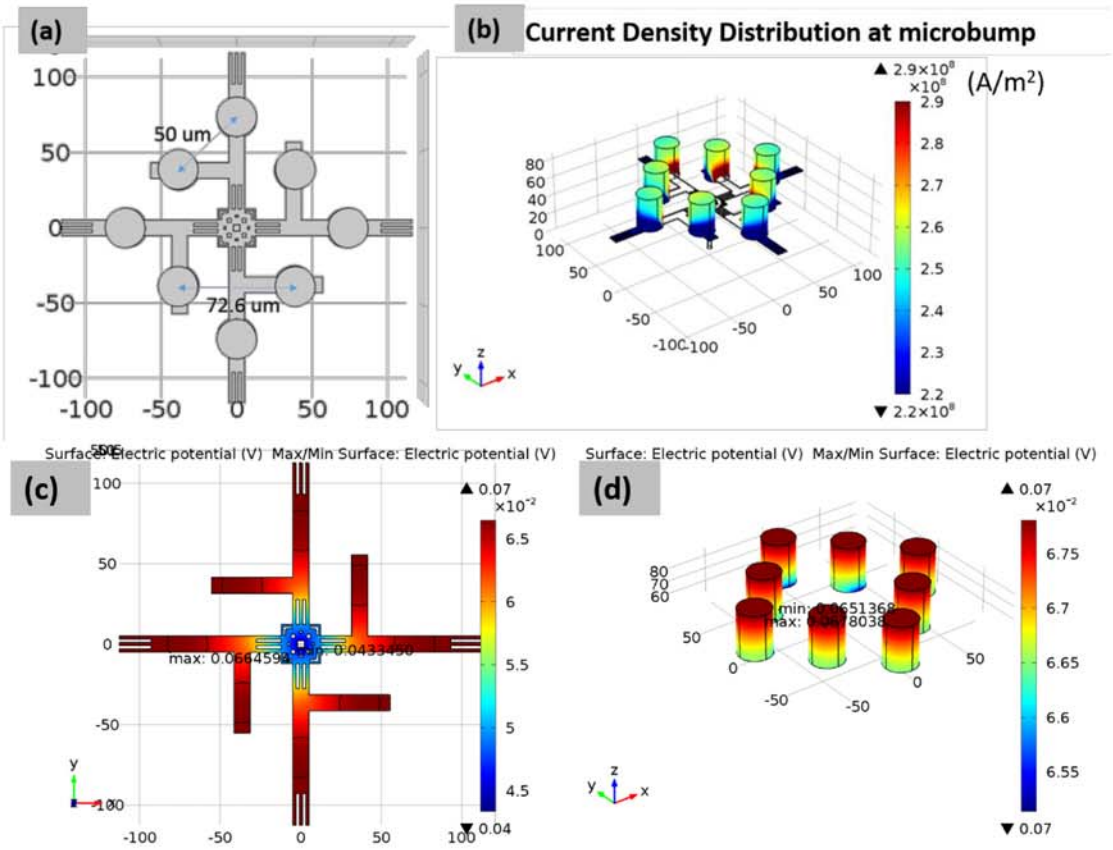

Fig. 3.6 Front-Side Design and Current Density Distribution by Considering Current Crowding Effect (a)Top View; (b) Current Density Distribution of μ-bumps; (c) IR drop of front-side fat wire level; (d) IR drop of μ-bumps.

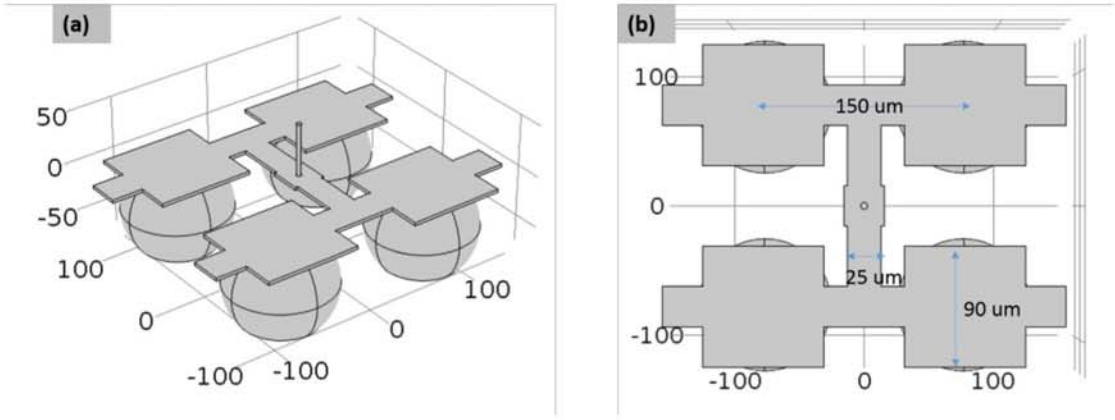

Fig. 3.7 3-D and Top View of Back-Side Design.

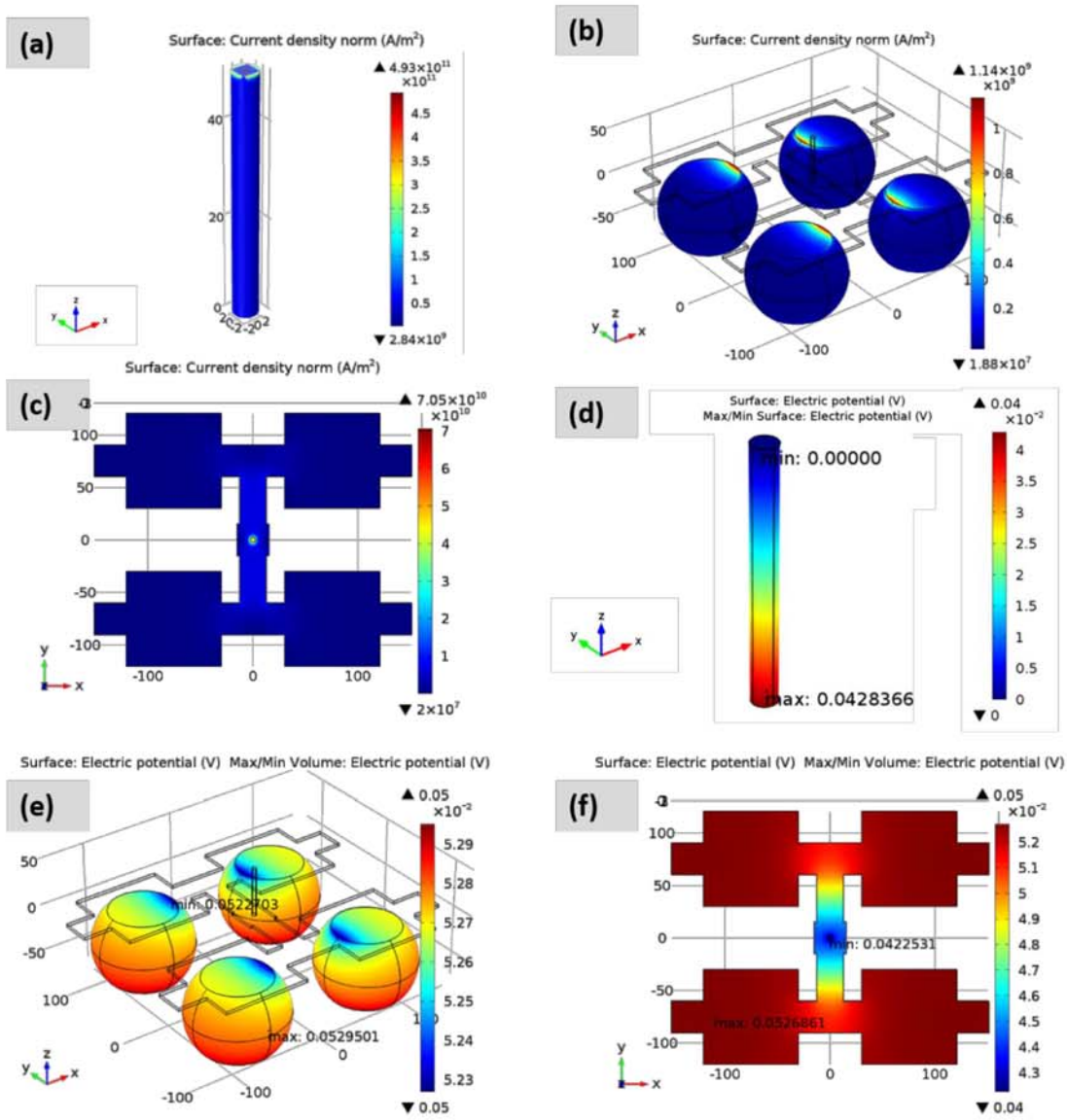

Fig.3.8 Current density distribution and IR drop of backside component.

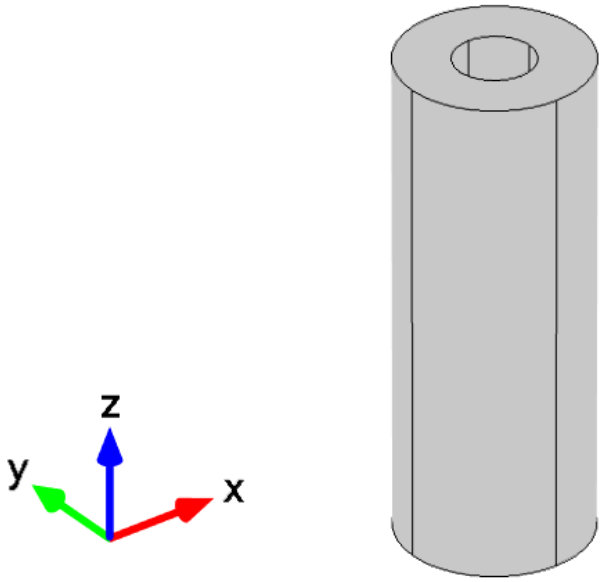

Fig. 3.9. Schematic of annular TSV.

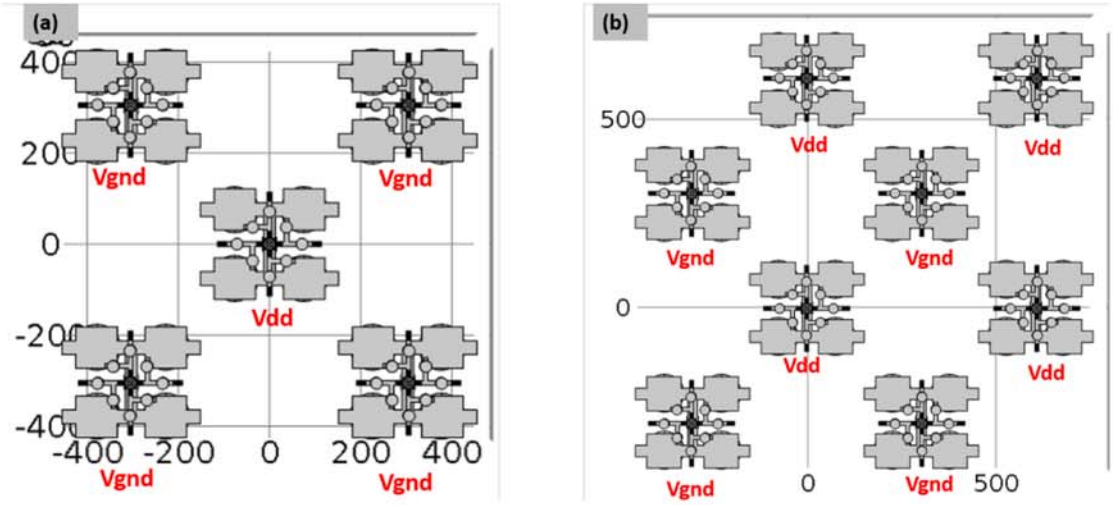

Fig. 3.10 Power Delivery Network Lattice Structure.

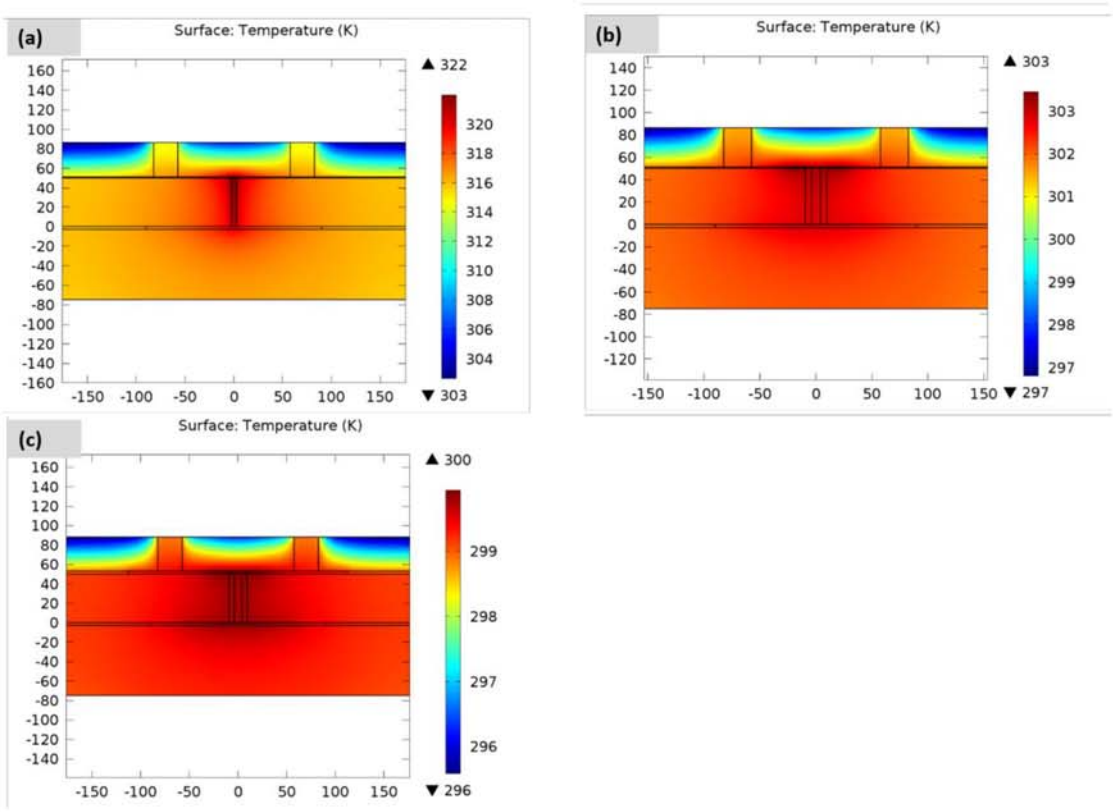

Fig. 3.11 Temperature distribution using (a) cylindrical TSV with fat wire. (b) annular TSV with fat wire; (c) annular TSV with superfat wire.

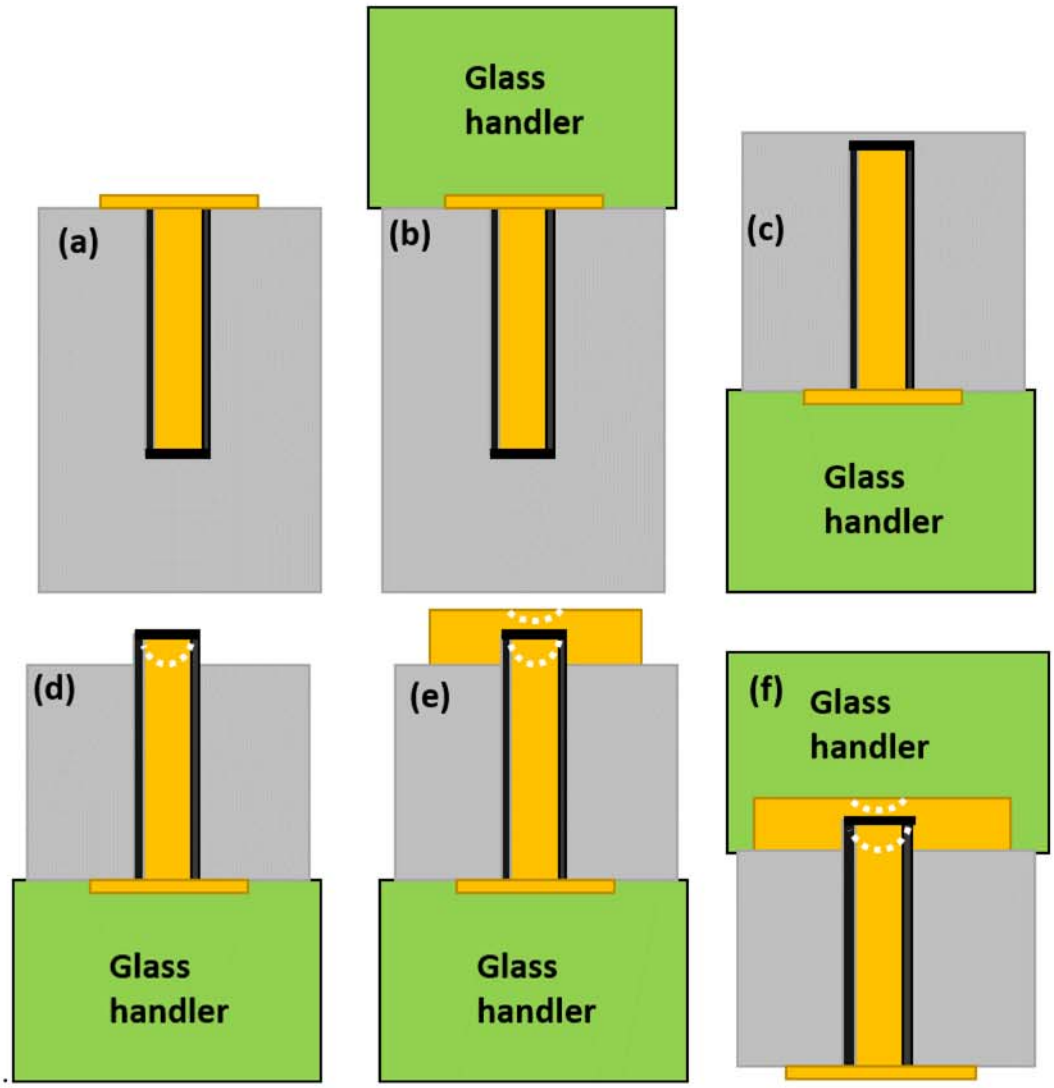

Fig. 3.12 TSV manufacturing process (a) Via filling; (b)-(c) back side grinding; (d) TSV exposure; (e) grind-side RDL deposition; (f) Grind side glass handler attach.

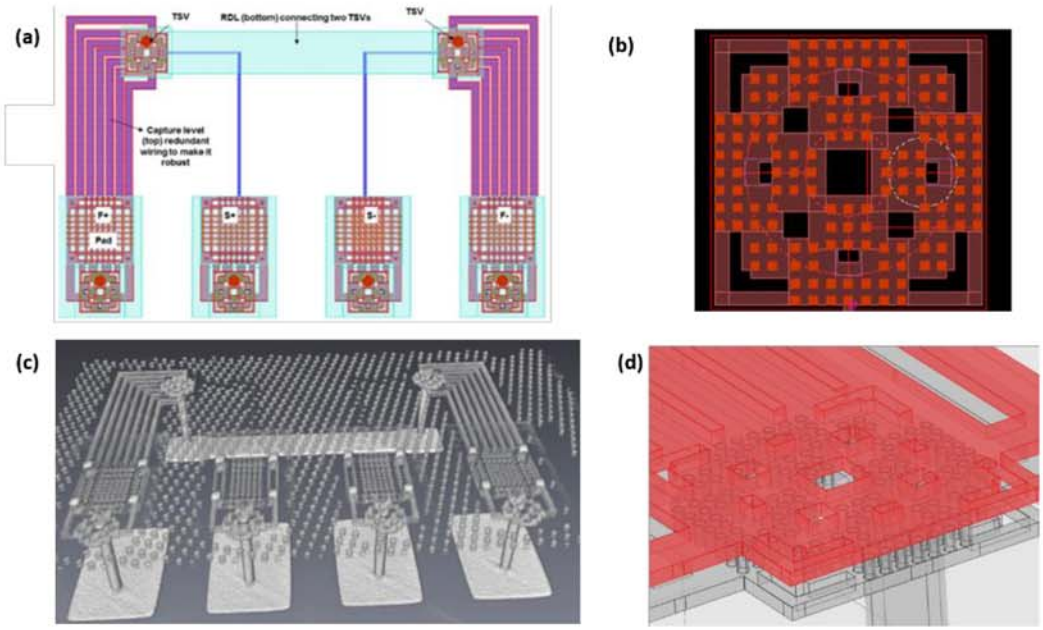

Fig. 3.13 Testing vehicle circuit. (a) Schematic of testing circuit; (b) Schematic of cheesed pad; (c) Synchrotron X-ray tomography image of the as-received state of the circuit; (d) Magnified schematic showing two level fat wire.

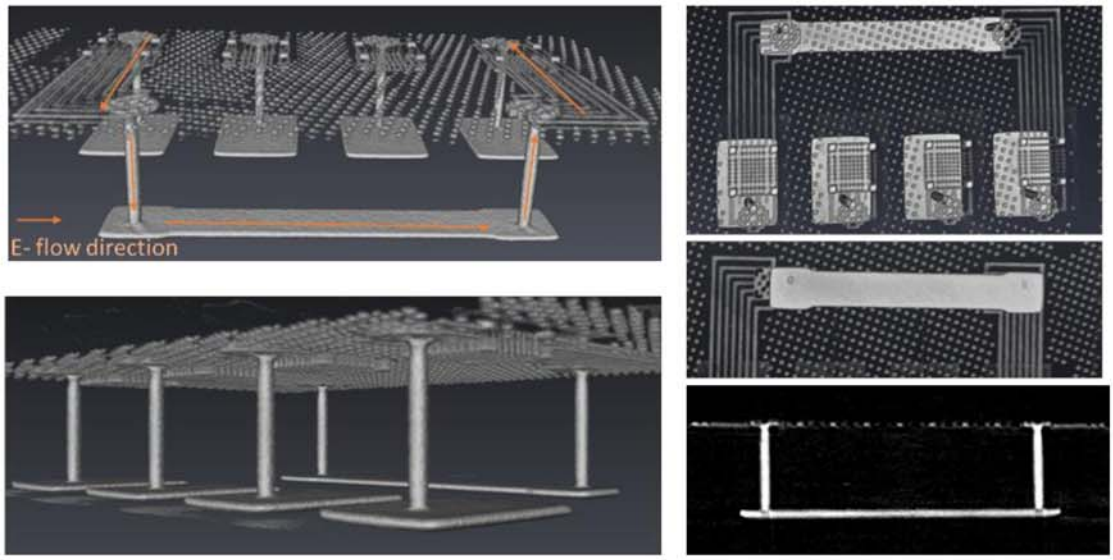

Fig. 3.14 Testing vehicle as-received state. (a) 3-D image of testing structure; (b) TSV; (c) front-side RDL; (d) grind-side RDL; (e) cross-section image.

Fig. 3.15 (a) testing structure showing wire bonding. (b) open failure at cathode after EM test.

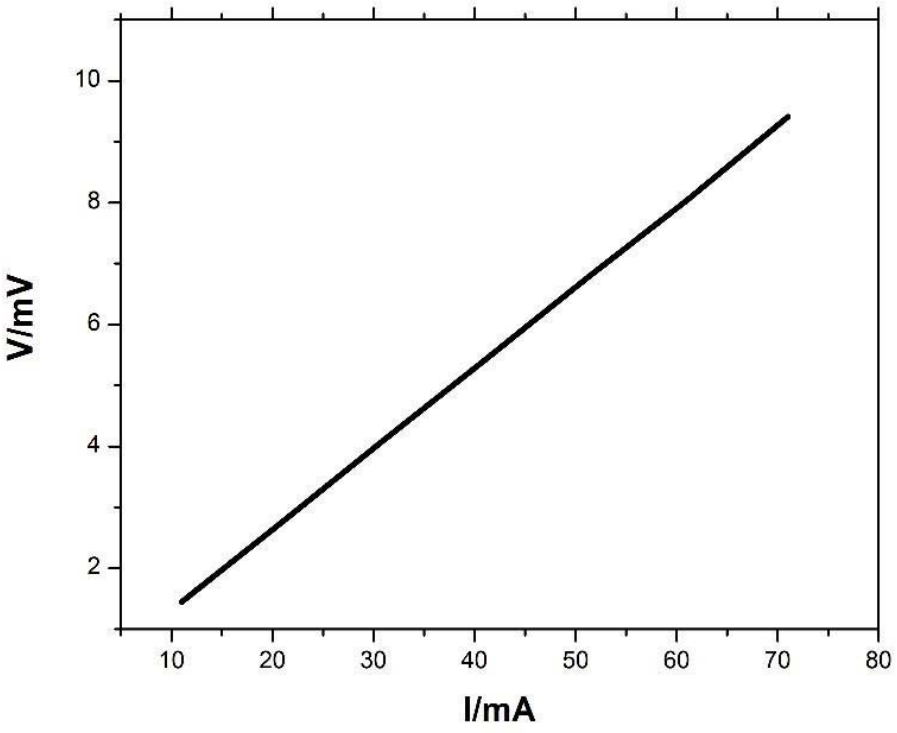

Fig. 3.16 I-V curve before EM test.

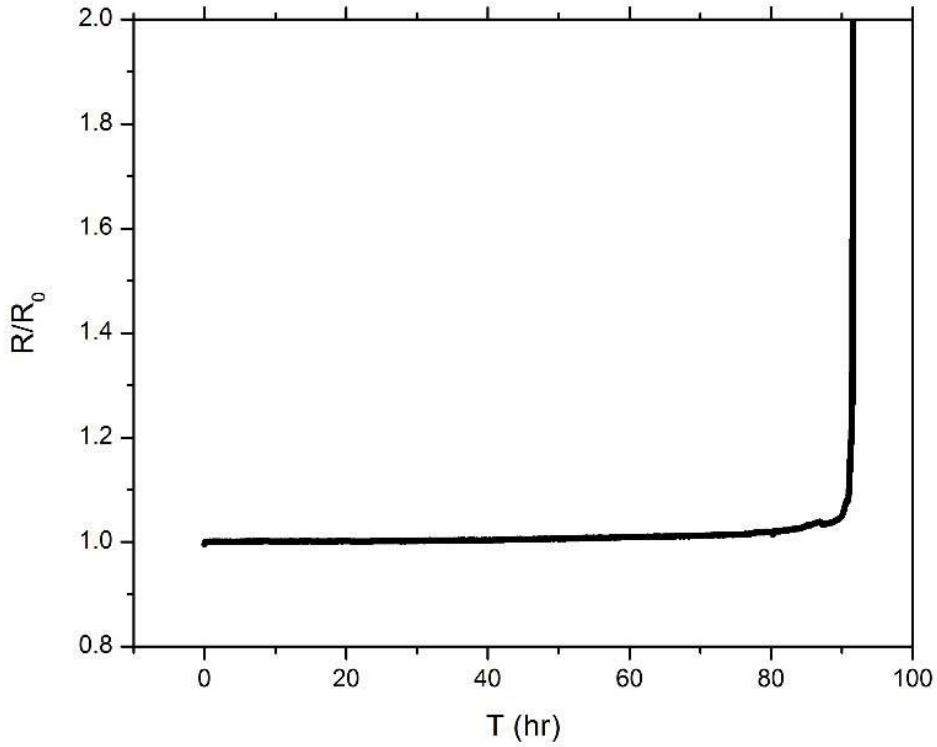

Fig. 3.17 Resistance-time plot.

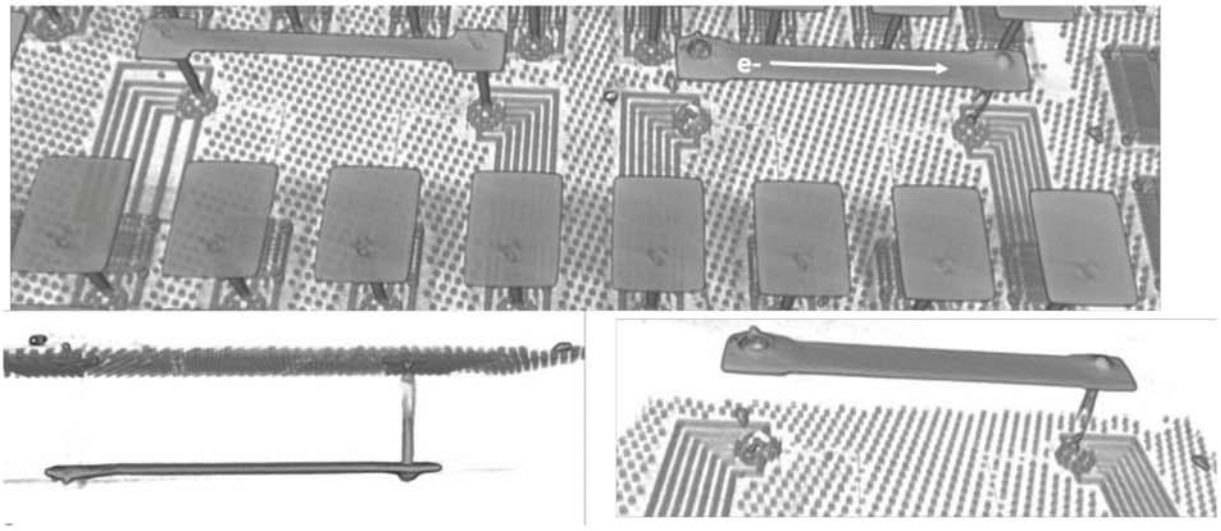

Fig. 3.18 Testing structure after EM open failure. (a) 3D testing circuit with reference circuit after EM failure; (b) cross-section; (c) magnified image showing extrusion and depletion.

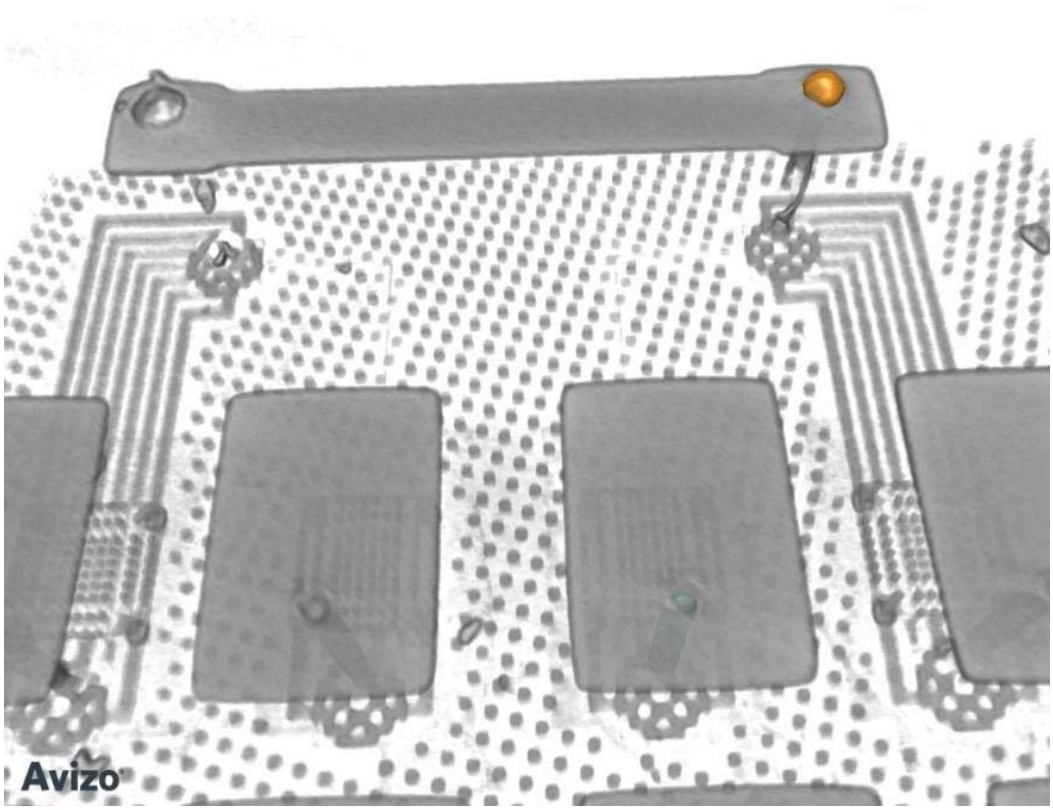

Fig. 3.19 Quantitative analysis of volume of the extrusion (highlighted area).

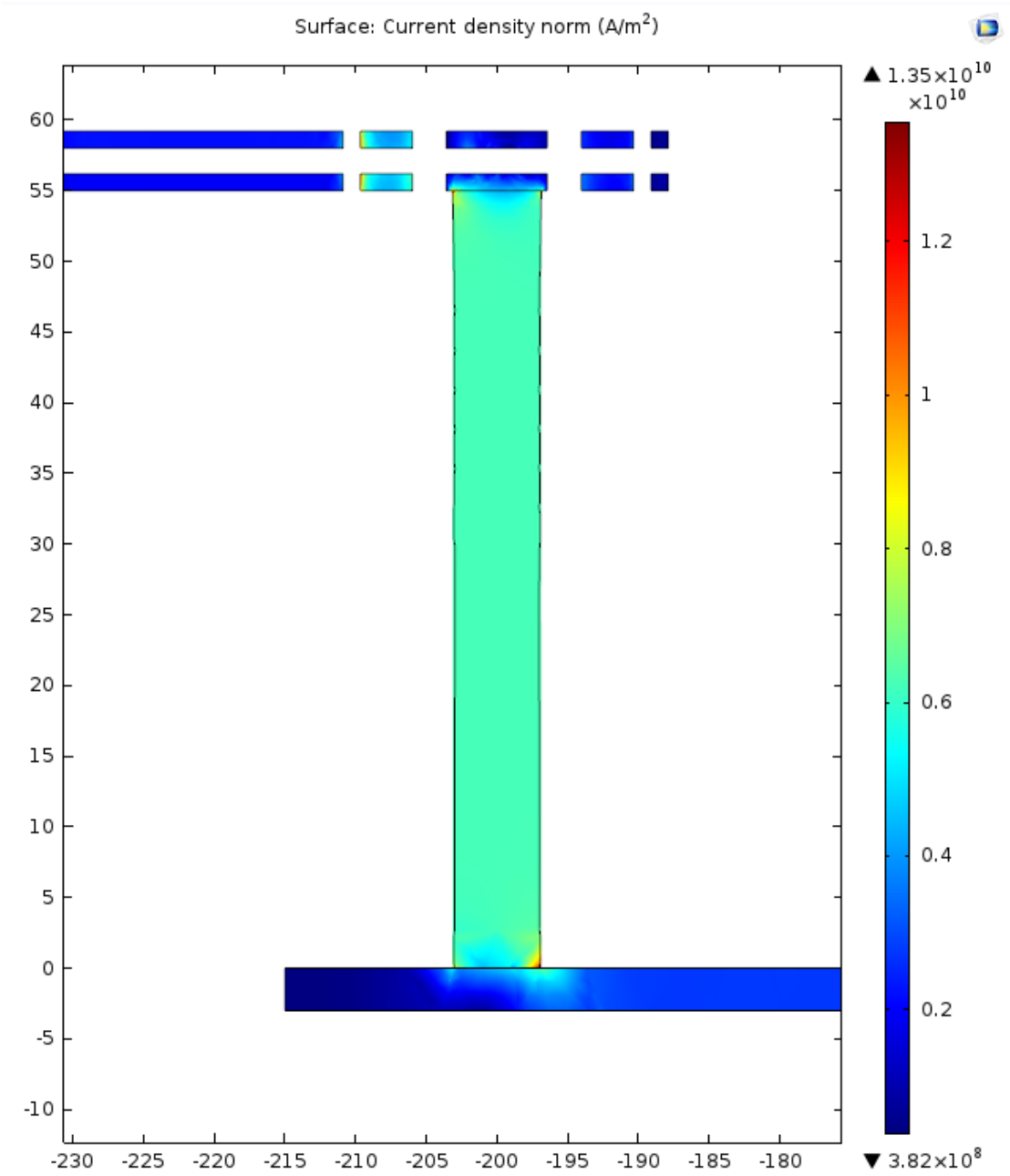

Fig 3.20 Simulation result of current density distribution.

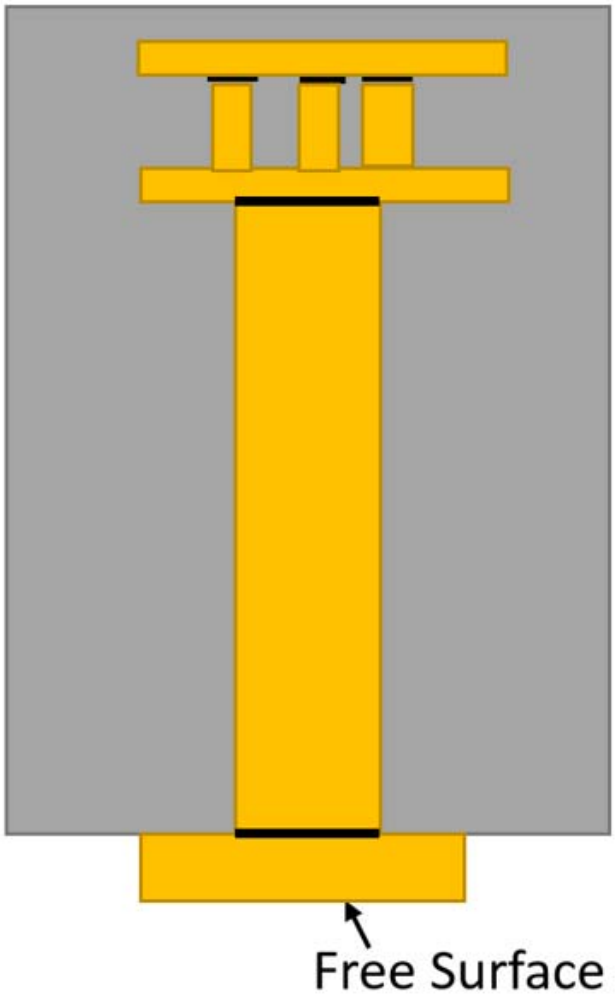

Fig. 3.21 Schematic showing diffusion barrier (dark line), and free surface.

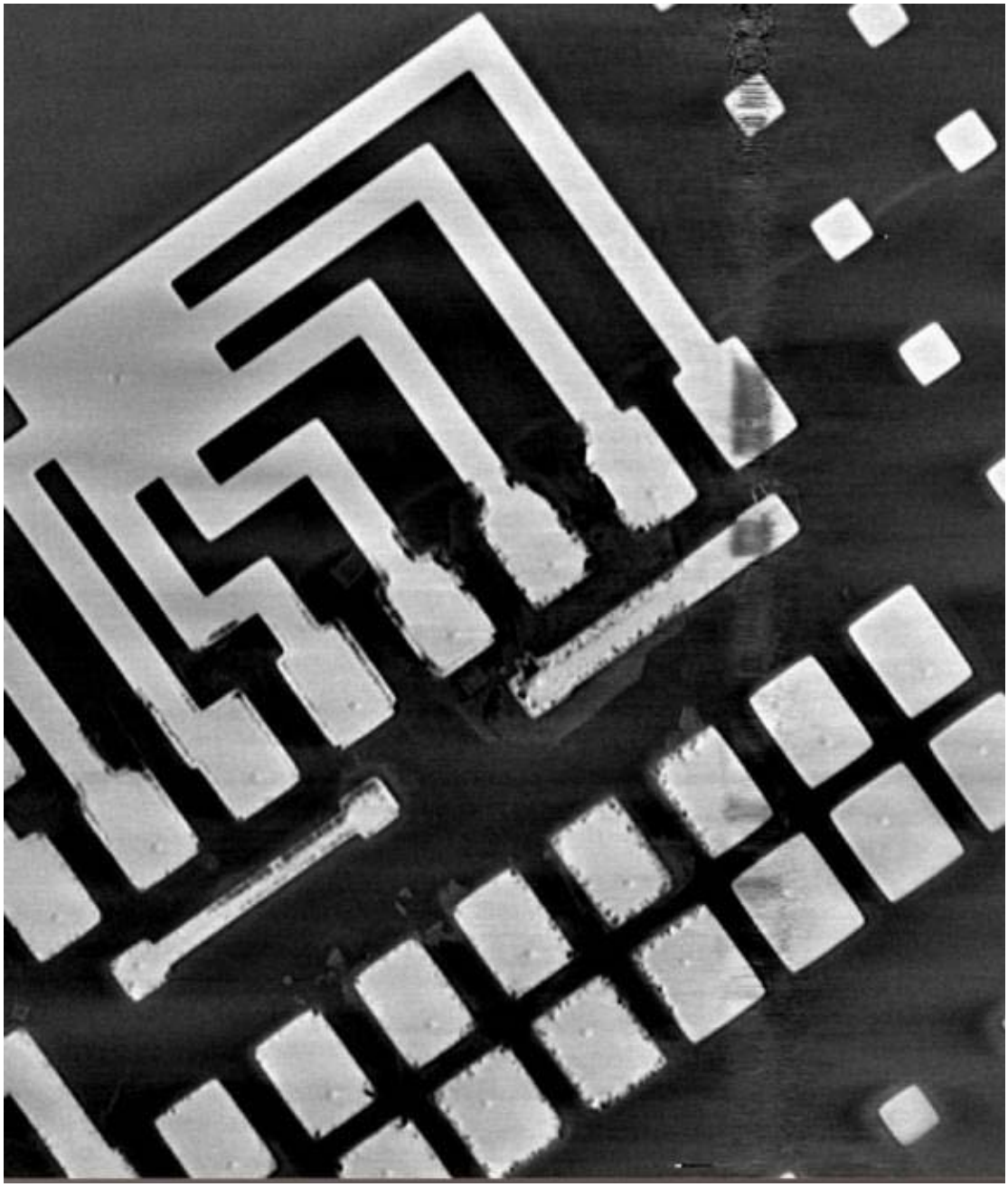

Fig. 3.22 Synchrotron X-ray image showing roughness of grind-side RDL.

Table 3.1 Current carrying capability of TSV, C4 bump and μ-bumps.

	TSV(Cu)	C4 Bump (Sn)	μ-bump (IMC)
Diameter (μm)	5	100	25
Maximum Current (A)	1- 1.5 [9]	~0.25 [10]	0.14-0.68 [11]

Table 3.2 Materials properties used in simulation.

Materials	Electrical Conductivity [S/m]	Thermal Conductivity [W/(m▪K)]	Heat capacity (J/(kgK))
Cu	5.88 e7	398	385
Sn	8.7 e6	73	227
Cu6Sn5	5.7 e6	34.1	286
Underfill	1.0 e-6	1.3	1700
Si	1.0 e-12	149	710
SiO2	1.0 e-14	1.38	703

Table 3.3 IR drop of each component (Assume I=1A).

Interconnects	Cylindrical TSV with fat wires		Annular TSV with fat wires		Annular TSV with "super-fat" wires	
	IR drop (V)	Percentage (%)	IR drop (V)	Percentage (%)	IR drop (V)	Percentage (%)
μ-bump	0.002	2.7%	0.002	5.0%	0.002	8.6%
Front-side fat wire level	0.023	30.4%	0.023	57.9%	0.0065	28.0%
TSV	0.04	52.8%	0.004	10.1%	0.004	17.2%
Grind-Side RDL	0.01	13.2%	0.01	25.2%	0.01	43.2%
C4 bumps	0.0007	0.9%	0.0007	1.8%	0.0007	3.0%
Total	0.0757	100%	0.0397	100%	0.0232	100%
Total reduction (%)	--		48%		70%	

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Chapter 4 Thermo-crosstalk induced failure for the un-powered microbumps

4.1 Introduction

In Chapter 2 and Chapter 3, we are discussed vertical Joule heating induced Electromigration failure in RDL and TSV. In the 3D IC, microbump is another vertical interconnection, and the Si interposer will also conduct heat laterally. Today, the diameter of microbumps is below 20 μm, and the entire microbump will become mostly intermetallic compound (IMC) after reflow[1,2]. Previous work on the reliability of microbumps has studied the mechanical property of IMC[3,4], and compared the electromigration (EM) and thermomigration (TM) resistance of IMC to lead-free solder[5,6,7]. To our best knowledge, there is no report on Joule heating induced damage on the neighboring un-powered microbumps due to thermal crosstalk. In this work, we investigate the reliability of the microbumps in the un-powered chip next to a powered chip. We note that these two chips are not stacked one above the other, rather they are placed neighboring each other horizontally on a Si interposer. Due to thermal cross-talk, the lateral heat transfer of Joule heating has generated an unexpected thermomigration failure in this mode of 2.5D IC integration. We have compared the EM effect on the powered microbumps, and the Joule heating induced TM effect on those microbumps in a neighboring un-powered chip. Furthermore, we have also compared both the EM and TM damages to a constant temperature thermal annealing at microbumps without temperature gradient or electrical current.

4.2 Experimental procedure

Fig. 4.1 (a) and 4.1 (b) show respectively an SEM cross-sectional image and an x-ray tomography image of the top view of our test sample. In the test structures, there are two levels of Si chips; the bottom Si chip serves as an interposer, and connected to the top two Si chips through thermo-compression bonded microbumps. The top two Si chips are placed horizontally, and separated by the underfill materials. The circuit of the microbumps is shown in Fig. 4.1 (c). Under each chip, there are two daisy chains of microbumps with 17 μm in diameter and 30 μm in pitch. In our EM test, one daisy chain of the microbumps under the right-hand chip (Chip 2) is stressed under current density of 5.3×10^4 A/cm^2. The testing temperature is 150 ℃ and 170 ℃.

Owing to the Joule heating in the daisy chain, the temperature in the powered microbumps will have a temperature about 30 ℃ above the ambient temperature. Yet we note that there is no temperature gradient in the powered microbumps (dashed line) in chip 2. So the powered microbumps have EM but no TM.

As one daisy chain in Chip 2 is powered, the Joule heating will transferred to the un-powered microbumps in the neighboring chain in Chip 2 through both the top Si chip and the bottom Si interposer. Therefore, the un-powered microbumps in Chip 2 have no thermal gradient, but they will experience a constant temperature annealing, slightly higher than the ambient temperature due to Joule heating, but no EM and TM.

More importantly, due to heat transfer horizontally from Chip 2 to Chip 1 through the interposer, but not through the underfill, it will make the bottom part of the un-powered microbump hotter than the top part. In turn, it creates a temperature gradient in the un-powered microbump under Chip 1. If the temperature gradient is large enough, TM occurs. This did happen in our test samples.

In summary, we have three different sets of microbumps in our test structure: microbumps under EM (the powered microbumps in Chip 2), microbumps under TM (microbumps in Chip 1), and microbumps under thermal annealing (the un-powered microbumps in Chip 2). Thus, this test structure is much more comprehensive than those in the previous studies, and it could provide a good comparison among different reliability mechanisms.

Fig. 4.2 shows the daisy chain in our test sample, with 4.2(a) the cross-sectional view through SEM and 4.2(d) the top view through X-ray micro-tomography. We note that the connection (rectangle 1) at the top is by Al, and the connection (rectangle 2) at the bottom is by Cu, as shown in Fig. 4.2(a). However, the connection through the bumps is very small, as shown in Fig. 4.2(d). We used FIB to cut a cross-section to view the dimension of the small connection, as shown in Fig. 4.2 (b), and 4.2 (c). Specifically, the Cu bridge has a depth of 1 μm, while the Al bridge has a depth of 3 μm. Under the applied current, the current density in the Cu bridge is 1.2×10^7 A/cm^2 while the current density in the Al bridge is 3.2×10^6 A/cm^2. The current density is high enough to cause electromigration in Cu and Al bridges. Therefore, the electromigration failure is also possible in these small connections..

The microstructure and composition were examined by using the Nova NanoSEM™ scanning electron microscope (SEM) and energy dispersive spectroscopy (EDS), respectively. The statistical comparison and three-dimensional view of the damage in the three sets of microbumps are conducted through non-destructive synchrotron radiation (SR) x-ray micro-tomography at Beamline 8.3.2 of the Advanced Light Source at Lawrence Berkeley National Laboratory.[8] An X-ray energy of 35 keV was used, and 1025 images were collected as the sample was rotated over 180 degrees. A 50 micron LuAG scintillator was used with a 10x lens in an optical system from Optique Peter, with a PCO.edge camera, yielding a pixel size of 0.65 microns/pixel. The tomographic reconstruction was carried out using Octopus, and visualization and analysis was carried out in the FIJI/ImageJ and Avizo software packages.

Before the EM test, the microstructure of the microbump in the as-received state is analyzed. Fig. 4.3(a) shows 3D image of one row of the microbumps in the as-received state by X-ray micro-tomography, while Fig. 4.3(b) is the 3D image of one microbump by the same technique. In the Fig. 4.3(a) and 4.3 (b), the purple-blue layer is the solder layer, from which we can see that there is no obvious solder extrusion and no filler trap in all the microbumps. Fig. 4.3(c) is the SEM cross-sectional image of the microbump in the as-received state. The materials in the microbump are indicated in the image. The structure is Cu/Ni/Cu/solder/Ni/Cu. We note that there is a thin layer of Cu coated between the top Ni layer and the solder layer in the as-fabricated state. After thermal compression bonding, the EDS result (Fig. 4.3(d)) shows that the IMC of both the Cu and Ni end of the solder layer is Cu_6Sn_5. And there is still remaining Sn in the solder layer. Because we are more interested in the failure

mode of the IMC. we annealed the sample at 170 ℃ for four days to consume all the Cu before EM testing.

Interestingly, after annealing for four days (Fig. 4.4(a)), all of the IMC will transform from Cu_6Sn_5 to $(Cu,Ni)_3Sn_4$ indicated in the EDS result (Fig. 4.4(c)). This is because thermodynamically $(Cu,Ni)_3Sn_4$ is more stable than Cu_6Sn_5. Fig. 4.4(b) shows the microbump after 285 hours annealing at 170 ℃, from which we can see (Cu,Ni)3Sn4 is stable for further annealing, and the amount of Sn will gradually decrease by reacting with Ni at both ends. After 285 hours annealing at 170℃, the solder layer became almost fully IMC. There are no voids and no sidewise diffusion of Sn for this high temperature storage testing. This indicates that the volume shrinkage from phase transformation in this structure is not serious to cause significant void formation.

After annealing (four days), we passed current (120 mA) to one of the daisy chain in Chip 2. Fig. 4.5 shows the I-V curve before EM test. The initial resistance is about 45 Ω at room temperature. During EM testing, we monitor the voltage continuously with time until the circuit is open. Fig. 4.6 is one of the resistance-time plots testing at 150 ℃. The resistance increased slowly first, and then jump abruptly before failure, which is typical for electromigration. In our EM tests, all the open failure has the same resistance-time behavior as shown in Fig. 4.6. Some other tests are stopped before the open failure in order to examine the microbumps in the middle stage.

4.3 Failure Results

To determine the weak link of the system where the early failure has occurred, we examined the Cu bridge, Al bridge, and the three kinds of microbumps after failure. The SEM images of these components are shown in Fig. 4.7. The materials and the electrical current flow direction are indicated in the image. We can see that the Al bridge (Fig. 4.7(a)) has voids along the grain boundary while Cu bridge (Fig. 4.7(b)) has small void at the surface. This indicated that the open circuit in our test structure might fail in the Al bridge. More interestingly, there is Sn diffusion out from the solder layer and react with the Ni barrier layer, and Cu Under Bump Metallization (UBM) in all the three kinds of the microbumps. Specifically, the sidewall diffusion of Sn in the EM bump transforms the IMC from Sn-rich $(Cu,Ni)_3Sn_4$ phase to Sn-poor phase $(Cu,Ni)_6Sn_5$ on the side of the solder layer. The Sn sidewall diffusion from the region of pure Sn (referred to Fig. 4.4(a)) will leave voids in the solder layer. The voids might link together and form a big void, as shown in Fig. 4.7(c). The damage in the powered microbumps is as expected. But what is more surprising is that the microbumps in the un-powered neighboring chip which undergoes TM has a much more serious damage than the powered microbumps. As we can see from Fig. 4.7(d), the microbumps under TM has much more sidewall diffusion of Sn, and there are much bigger voids within the solder layer.

We also compared the un-powered microbumps that are under thermal annealing, but the temperature of these microbumps is slightly higher than the EM bumps because these micropbumps are heated from both sides. For example, the 2nd

row of the microbumps (un-powered) is heated from both the 1st row and the 3rd row of the powered microbumps. The damage in the thermal annealing bump is shown in Fig. 4.7(e). We can see that the thermal annealing microbump also has sidewall diffusion and void formation. But the damage is much less than the microbumps that are under TM.

In order to understand the formation and development of these voids, the following experiments were performed to examine the un-powered TM microbumps during the EM test at different stages before the circuit fails. Because initially the void is not big enough to be seen clearly by SEM, focused ion beam (FIB) is also used to cut through the microbumps to see the voids distribution. We also compared these un-powered TM microbumps with the EM microbumps and the microbumps that are under thermal annealing in the middle stage. Fig. 4.8(a) and 4.8(b) shows the SEM and FIB images of the microbumps under TM after 2 days when the applied current is also 120 mA, and the temperature is 170 ℃. We can see that there are small voids nucleated at the top of the solder layer, which is the cold end. This indicates that the lattice diffusion of Sn in the IMC under thermal gradient is from the cold end to hot end, which agrees with the data in the literature. [9,10] Also, we notice that there are relatively larger voids in the middle which corresponds to the area with pure Sn after annealing. The void formation here indicates that pure Sn has less resistance to TM than the IMC. Meanwhile, the side of the solder layer has more mass depletion, this is because of faster surface diffusion along the sidewall than the lattice diffusion. After 3 days powering, the un-powered microbumps under TM were examined by SEM. Fig. 4.9(a) and 4.9(b) are the SEM images of two microbumps, from which we can see that the big voids are still in the middle, but the small voids in the top part has

increased in number and grown bigger in size. In flip chip solder joints, the TM phenomenon has been well studied, and the literature agrees that under a thermal gradient higher than 1000 ℃/cm, the TM will occur. [11,12] This means only a temperature difference of 0.7℃ between the top and the bottom of solder layer will have TM effect in our microbumps, and this temperature difference is very small. In the next section, we will simulate the temperature gradient in the solder layer, and confirm that the temperature gradient in the solder layer is greater than 1000 ℃/cm.

The powered EM microbumps and the thermal annealing microbumps are also examined in the middle of the EM test, which can provide a good comparison. Fig. 4.10(a) and 4.10(b) are the EM bumps that are powered two days at 170℃. The circuit is not failed yet, while Fig. 4.10(c) is the un-powered microbump (annealing bump) that is at the same die, but at a slightly higher temperature due to Joule heating. We can see that the void distribution is not obvious in these three bumps as in the TM microbumps. The void size and volume is much smaller than those in the TM microbumps. There is a slight polarity effect in the EM bumps, with more Ni consumption in the lower side in the downward electron flow direction, while more Ni consumption in the upper side in the upward electron flow direction. This is even clearer with longer powering time. Fig. 4.11(a) and 4.11(b) are the EM microbumps that were powered at 170 ℃ for 76 hours. The polarity effect of the Ni UBM consumption is much clearer. In Fig. 4.11(a), when the electrons flow upward, there is much more Ni consumption in the upper end compared with that in Fig. 4.11(b). However, when the electrons flow downward (Fig. 4.11(b)), the Ni consumption in the bottom end is much more than that in Fig. 4.11(a). This polarity effect indicates

that the electrical current has a strong effect on the lattice diffusion of Sn, and in turn the chemical reaction between Sn and Ni.

In this test structure, we powered more than ten rows of microbumps in each sample. It is unrealistic to polish and compare each rows using cross-sectional SEM. Therefore, synchrotron radiation x-ray micro-tomography was used to take 3D image of the whole structure to verify the phenomenon statistically. Fig. 4.12 shows one sample that is stressed at 120mA, 170 ℃ for 72 hours. Fig. 4.12(a) are the microbumps under Chip 2. Since we powered the microbumps in the odd rows under Chip 2, the microbumps in the even rows are under thermal annealing. Fig. 4.12(b) shows the microbumps under Chip 1. As we discussed before, these microbumps were under TM. From comparison, we can see that the microbumps that are under TM have had much more dimples on the surface of the solder layer, indicating that the surface diffusion of Sn in the TM microbumps are the most serious, and has caused more damages. For a better comparison, the magnified images of each set of the microbumps in the same sample of Fig. 4.12 are presented in Fig. 4.13. We can see from Fig. 4.13 that the surface damages of the TM microbumps are much more serious than the EM microbumps and the annealing microbumps. In order to check the damage inside the solder, the sample is analyzed slice by slice in the Avizo software. And we have created a movie to show each slice along the y-direction. From the movie, we can see that each slice indicates, even in the middle of the solder layer, the TM microbumps have at the least twice void volume than the EM microbumps and the annealing microbumps.

4.4 Discussion

4.4.1 Thermal Cross-talk

In 2.5D IC, the horizontal heat transfer through Si interposer is different from 2D IC. In the latter, the Si chips are placed horizontally on a polymer based laminate. This laminate has a low thermal conductivity (0.3W/(m·K) for FR4). If we power one circuit in one Si chip, the induced Joule heating will not be transported horizontally. However, in 2.5D IC, the Si chips are placed horizontally on a Si interposer. Since Si is a much better thermal conductor, with a thermal conductivity of 140 W/(m·K) (two orders higher than FR4), Joule heating will be transported easily through the interposer to the neighboring un-powered chip. This phenomenon is called thermal crosstalk. In order to verify quantitatively the damage due to thermal crosstalk, a three-dimensional simulation program was adopted to show the magnitude of temperature gradient in the microbump on the un-powered chip. Then the driving force of EM and TM are further calculated and compared.

The horizontal heat transfer in the Si interposer is first simulated to obtain the temperature at the hot end of the un-powered microbumps. The model is established by assuming Joule heating increased the temperature of the powered microbumps by 30℃. Then, the powered microbumps are modeled as a bulk with a fixed temperature of 180 ℃ (453 K) on a Si interposer. The surrounding temperature is assumed to be 150 ℃ (423 K). The result is shown in Fig. 4.14. In Fig. 4.14(b), the area of the TM bumps is marked with the initial point and the end point, from which we can see that the temperature at the hot end of the TM bumps is between 429 K to 436 K. In order

to simulate the worst case, we will use 436 K as the temperature of the hot end in the simulation. After knowing the horizontal temperature distribution, we simulated the vertical temperature distribution in the un-powered TM bumps as below.

Fig. 4.15 shows the geometry of the modeled unit. Here, the top Si chip has a thickness of 250 μm while the bottom interposer has a thickness of 760 μm. These two parameters are defined according to the sample geometry we received. Here we modeled three microbumps with different distribution of Sn in the solder layer to compare the difference. The geometry and the materials in the microbump is defined according to Fig. 4.4(a). The only difference is that we assume the IMC is Ni_3Sn_4, while in real cases there is Cu dissolution. The surrounding temperature is assumed to be 423 K. The top surface of the Si interposer (hot end) is assumed to be 436K, as shown in the highlighted part in Fig. 4.15(b). And the temperature of the bottom surface of the Si interposer, and the top surface of the Si chip which are exposed to the surrounding is assumed to be 150 ℃ (423 K), as shown in the highlighted part in Fig. 4.15(c).

The heat transfer in solid is governed by the following equation, [13]

$$\rho C_p \boldsymbol{u} \cdot \nabla T = \nabla \cdot (\kappa \nabla T) + Q \tag{4.1}$$

where ρ is the density, C_p is the heat capacitance, κ is the thermal conductivity, and $\boldsymbol{u}$ is distance over time step. Q is heat flux by the heat source or heat sink, in this case is the Joule heating. The materials property in this simulation is listed in Table 4.1.

Fig. 4.16 shows the simulation results of the temperature, and the temperature gradient of the microbumps. For the temperature gradient, we adjusted the color

legend and only show the one that is higher than 1000℃/cm. The three microbumps have different Sn distribution. In the solder layer, the left bump has Sn at the side of the IMC layer; the middle bump has Sn in the middle of the bottom of the IMC layer; and the right bump has full IMC in the solder layer. By comparison, we found that the different Sn distribution has little effect on the temperature distribution. But the existence of Sn in the solder layer will increase the temperature gradient around it. In addition, we found that the highest temperature gradient is in the IMC layer, and it is about 8000 ℃/cm. The Sn region in the solder layer also has high temperature gradient (around 5500℃/cm). This is because the IMC has a lower thermal conductivity, hence larger temperature gradient. Below we will compare the TM driving force with the EM driving force to confirm that such high temperature gradient can cause serious damage.

4.4.2 A comparison of the driving forces of TM and EM

To consider the driving force of TM, we assume that the atomic jump distance is $a = 3 \times 10^{-8} cm$, and take $\frac{\Delta T}{\Delta x}$= 5500 ℃/cm, we will have a temperature change of $1.7 \times 10^{-4}\ K$ across an atomic spacing, so the thermal energy change will be

$$3k\Delta T = 3 \times 1.38 \times 10^{-23} \left(J/K\right) \times 1.7 \times 10^{-4} K = 7 \times 10^{-27}\ J \qquad (4.2)$$

As a comparison, we shall consider the EM driving force, and the work done by the driving force in a distance of an atomic jump. [18] Because the EM parameter in solder is very well studied, we will only compare with pure Sn. We know that EM will occur in Sn when the applied current density is above 1×10^4 A/cm^2. The driving force for EM can be expressed as:

$$F = Z^* eE = Z^* e\rho j \tag{4.3}$$

We shall take $\rho = 10 \times 10^{-8}\Omega m, Z^* = 10, e = 1.6 \times 10^{-19}C$, and we have F=$1.6 \times 10^{-17}N$. The work done by an atomic jump will be $\Delta w = F \times a = 4.8 \times 10^{-27}$J. This value is slightly smaller than the thermal energy we calculated above. Therefore, if the current density of 1×10^4 A/cm^2 can induce EM in Sn, a temperature gradient of 5500 ℃/cm will definitely have TM damage in Sn. Indeed, the direct temperature measurement by IR technique in flip chip solder joint confirms that with a temperature gradient of 2571℃/cm, the thermomigration has occurred and driven Pb atom from hot end to cold end. [19]

4.4.3 TM and EM in intermetallic compounds

Tin has been reported to be less resistant to EM and TM than IMC because the chemical bonding in IMC is stronger and the diffusion is slower. [6,7] However, even if we annealed the microbumps for a long time and reacted all the remaining Sn with Ni to form IMC in the solder layer, the phenomenon of thermal crosstalk reported before still occurs. Fig. 4.17 shows two EM microbumps that are powered with 120 mA at 170 ℃ for 44 hours. Before the EM test, the sample is annealed at 170℃ for 285 hours to transform all the remaining Sn into IMC (Fig. 4.4(b)). We notice the polarity effect and the sidewall reaction which are similar to those in Fig. 4.11. Fig. 4.18 shows two TM microbumps in the same sample. From Fig. 4.18, we can see that the void also nucleated at the cold end, and the sidewall reaction of Sn with Ni and Cu UBM also occurred. This indicates that the thermal crosstalk phenomenon will play a

role even if the solder is fully converted to IMC. We notice that the temperature gradient in the IMC layer was predicted to be close to 8000 ℃/cm. Ouyang [20] reported that the TM in the IMC of Ni_3Sn_4 indeed will occur at 7308℃/cm by Ni diffusion from hot to cold end. However, in that paper, the Ni diffusion will not cause any void and damage, only the IMC growth difference. In our case, the Sn diffusion driven by temperature gradient causes much more serious effect.

4.5 Summary

The phenomenon of thermal-crosstalk between a powered and an un-powered Si chips on a Si interposer in a 2.5D IC circuit has been studied experimentally. It is confirmed by simulation of heat transfer of Joule heating from the powered chip horizontally along the interposer to the neighboring un-powered chip. The heat transfer creates a large temperature gradient, in the order of 1000 ^{o}C/cm, through the un-powered microbumps in the neighboring chip, so the microbumps failed by thermomigration. In our test structure, we have found other microbumps which were failed by electromigraion as well as by constant temperature annealing. We used synchrotron radiation tomography to compare the failure in these three kinds of microbumps: microbumps under electromigration, microbumps under thermomigration, and microbumps under a constant temperature thermal annealing. The results show that the microbumps under thermomigration have the largest damage. Our calculations showed that indeed the electromigration and thermomigration driving force are in the same order. The latter induced atomic flux of Sn to go from the cold end to the hot end, resulting in depletion and void formation at the cold end. Furthermore, the temperature gradient tends to enhance sidewall

surface diffusion of Sn to react with Ni and Cu. This sidewall surface diffusion of Sn can cause significant void formation in the solder layer in the microbumps.

Note: The materials of Chapter 4 was submitted to Journal of Applied Physics.

4.6 Figures

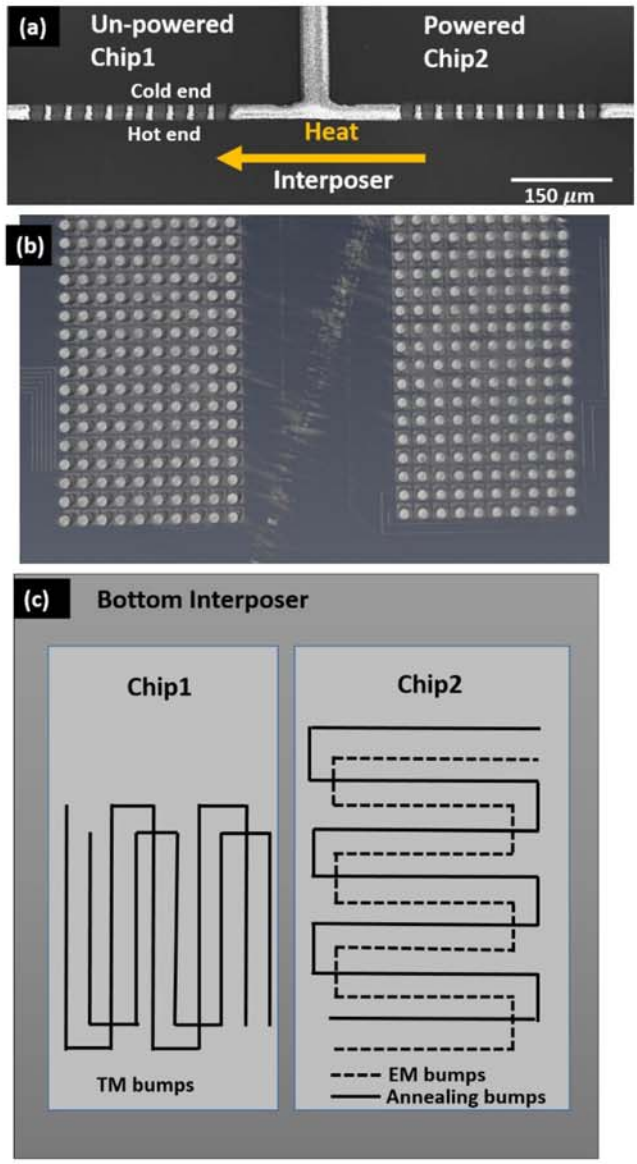

Fig. 4.1. Test sample (a) cross sectional SEM image; (b) top view by Synchrotron Radiation (SR) X-ray micro-tomography; (c) schematic of the circuit.

Fig.4.1(a) reprinted permission from (Menglu Li, Electromigration induced Thermomigration in Microbumps by Thermal Cross-talk across Neighboring Chips in 2.5D IC, IRPS) © 2016 IEEE

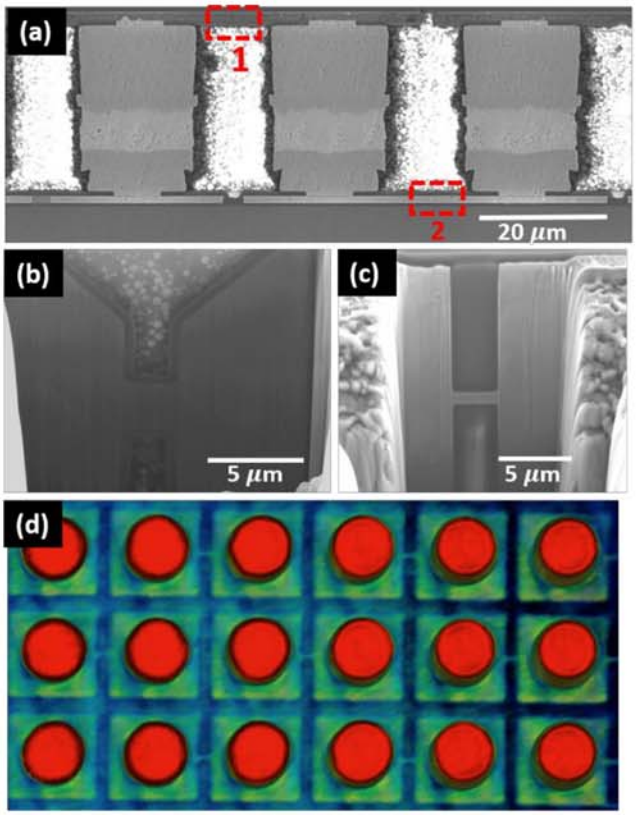

Fig. 4.2. Daisy Chain (a) cross sectional SEM image; (b) Al bridge; (c) Cu bridge (d) top view X-ray micro-tomography image showing Cu bridge.

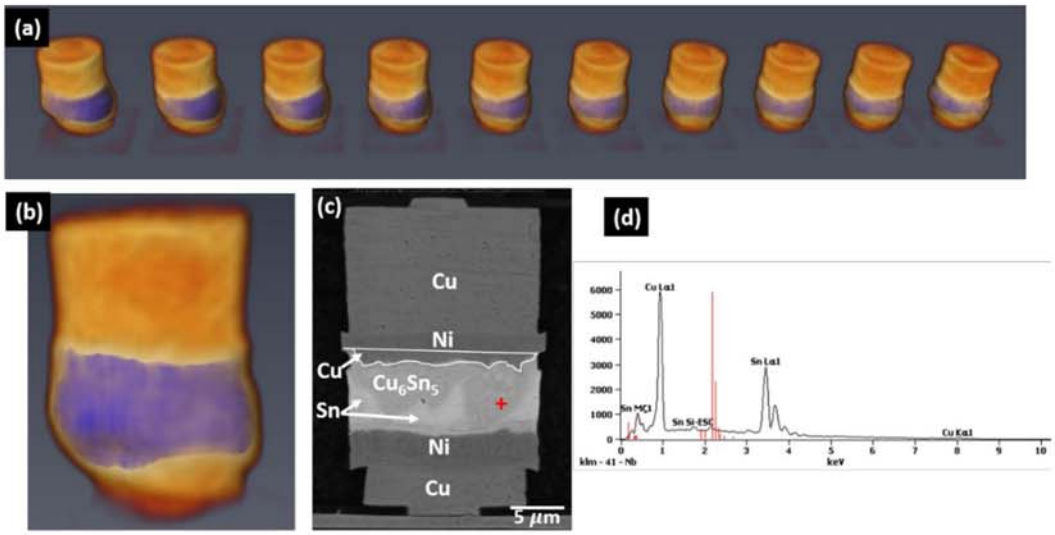

Fig. 4.3. Microbump in the as-received state (a) a row of (b) one of microbumps from X-ray micro-tomography;(c) SEM image of the cross-section (d) EDS spectrum at crosspoint.

Fig.3(c) and (d) reprinted permission from (Menglu Li, Electromigration induced Thermomigration in Microbumps by Thermal Cross-talk across Neighboring Chips in 2.5D IC, IRPS) © 2016 IEEE

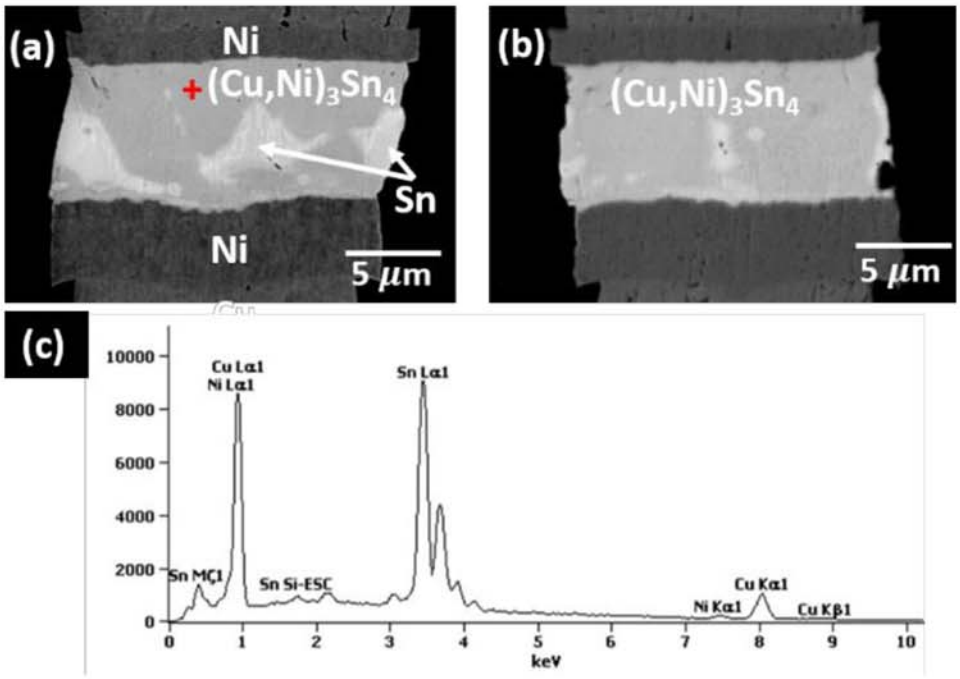

Fig. 4.4. Microbump after annealing (a) SEM image of the microbump annealed at 170 ℃ for four days; (b) SEM image of the microbump annealed at 170 ℃ for 285 hours; (c) EDS spectrum at crosspoint.

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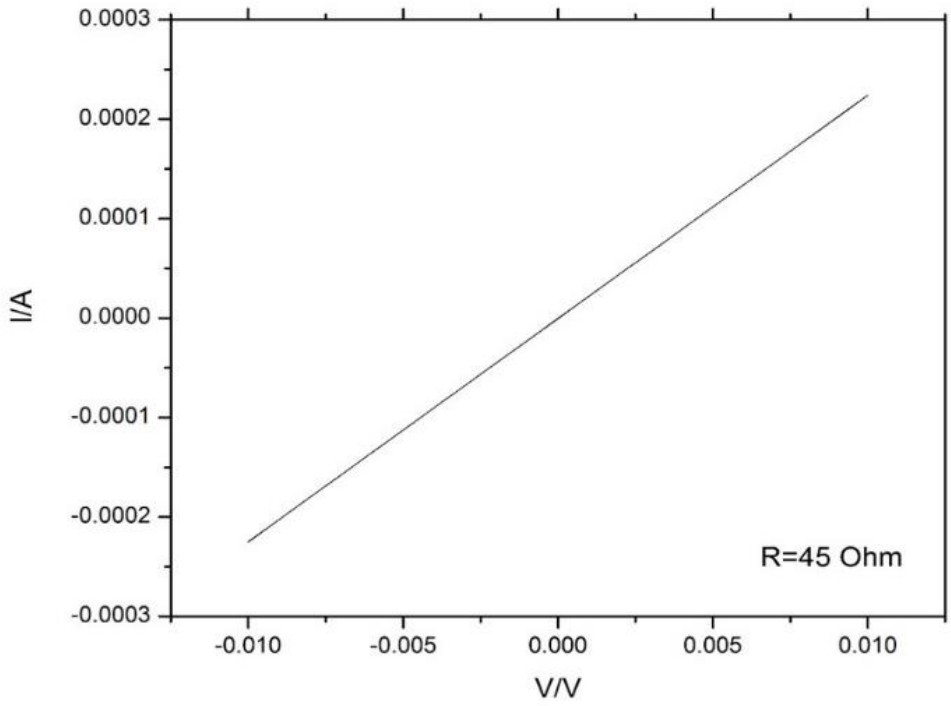

Fig. 4.5. I-V curve of the test circuit.

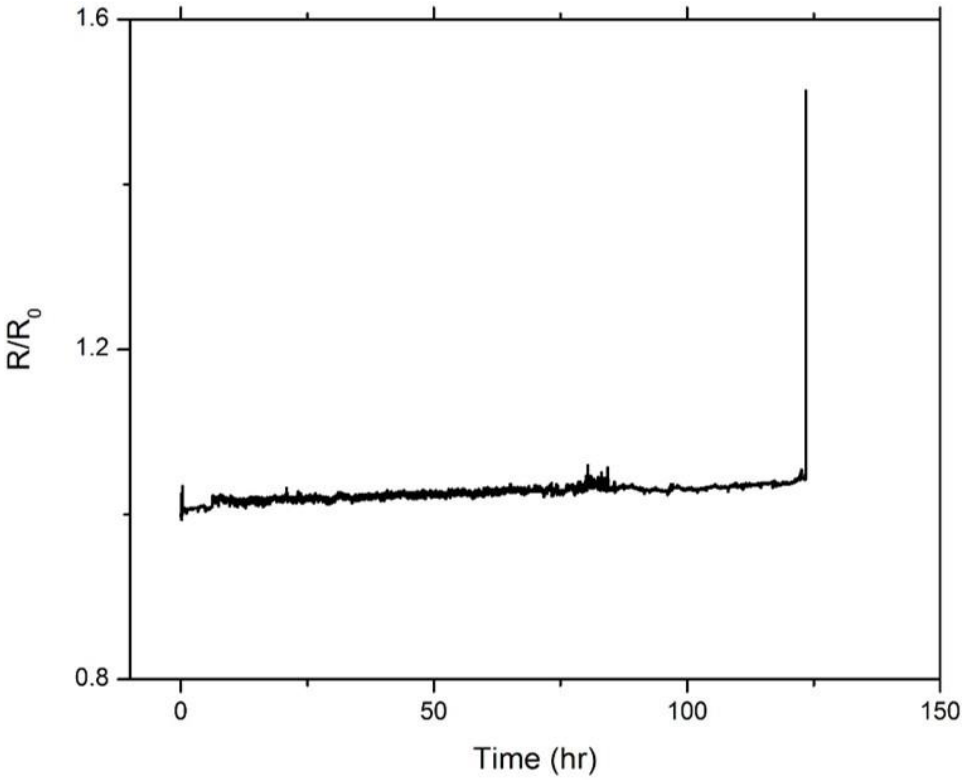

Fig. 4.6. The resistance change curves for one of the EM tests at 150 °C.

Fig.4.5 and Fig 4.6 reprinted permission from (Menglu Li, Electromigration induced Thermomigration in Microbumps by Thermal Cross-talk across Neighboring Chips in 2.5D IC, IRPS) © 2016 IEEE

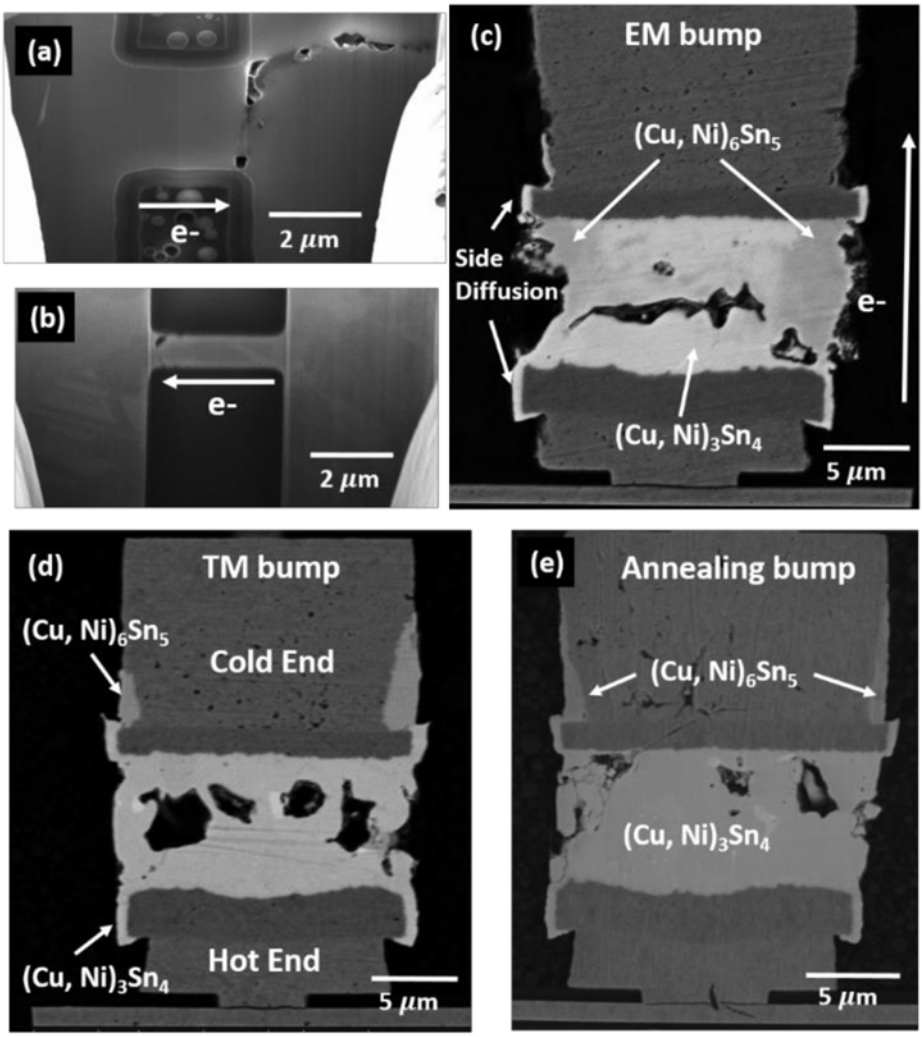

Fig. 4.7. SEM image of different component after 123.5 hours (open failure) at 150 ^{o}C (a) Al bridge; (b) Cu bridge; (c) microbump under EM; (d) microbump under TM; (e) microbump under thermal annealing.

Fig. 4.7(c) and (d) reprinted permission from (Menglu Li, Electromigration induced Thermomigration in Microbumps by Thermal Cross-talk across Neighboring Chips in 2.5D IC, IRPS) © 2016 IEEE

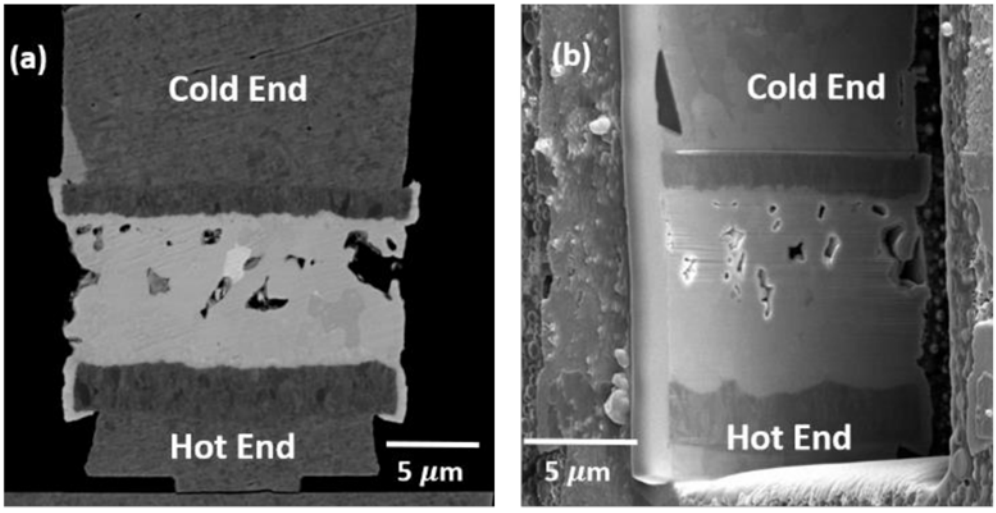

Fig. 4.8. SEM and FIB image of TM bumps after 48 hours powering at 170 ºC.

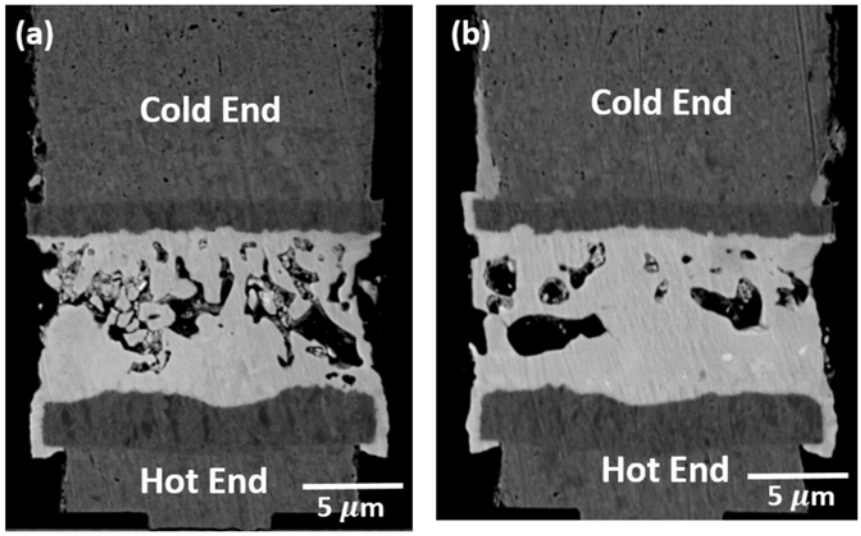

Fig. 4.9. SEM images of TM bumps after 72 hours powering at 170 °C.

Fig. 4.8(b) and Fig. 4.9 reprinted permission from (Menglu Li, Electromigration induced Thermomigration in Microbumps by Thermal Cross-talk across Neighboring Chips in 2.5D IC, IRPS) © 2016 IEEE

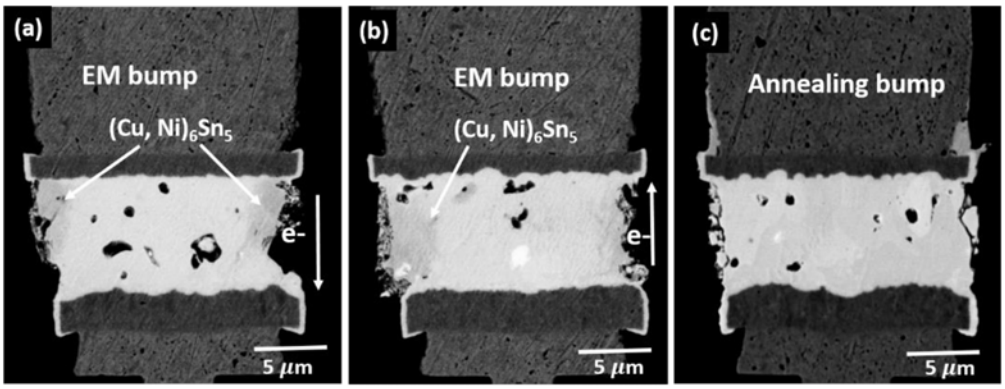

Fig. 4.10. SEM images after 48 hours powering at 170 ºC of
(a) downward EM bump; (b) upward EM bump; (c) annealing bump.

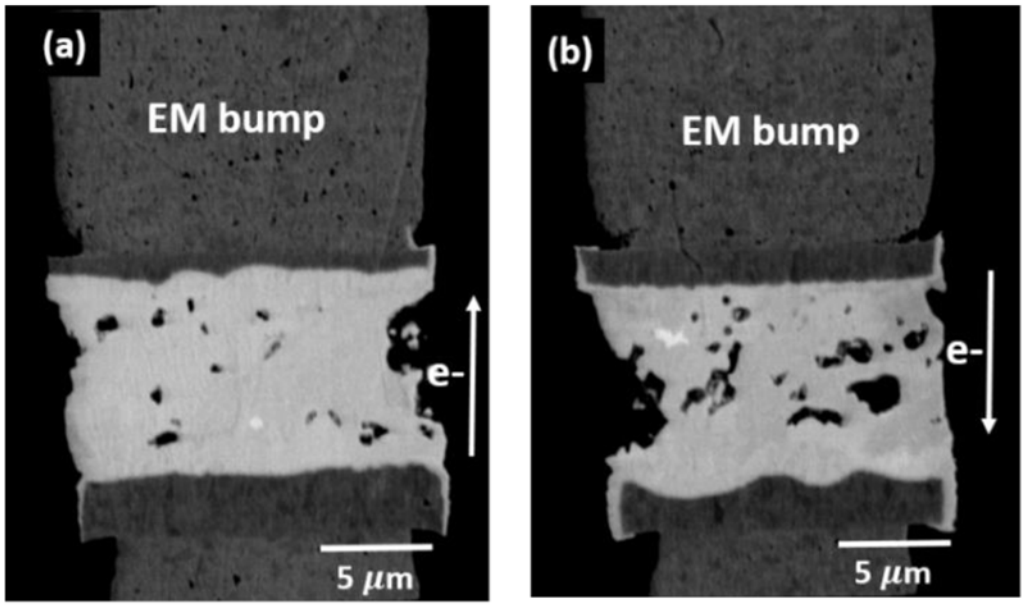

Fig. 4.11.SEM images of EM bumps powered at 170 ºC for 76 hours, (a) upward; (b) downward.

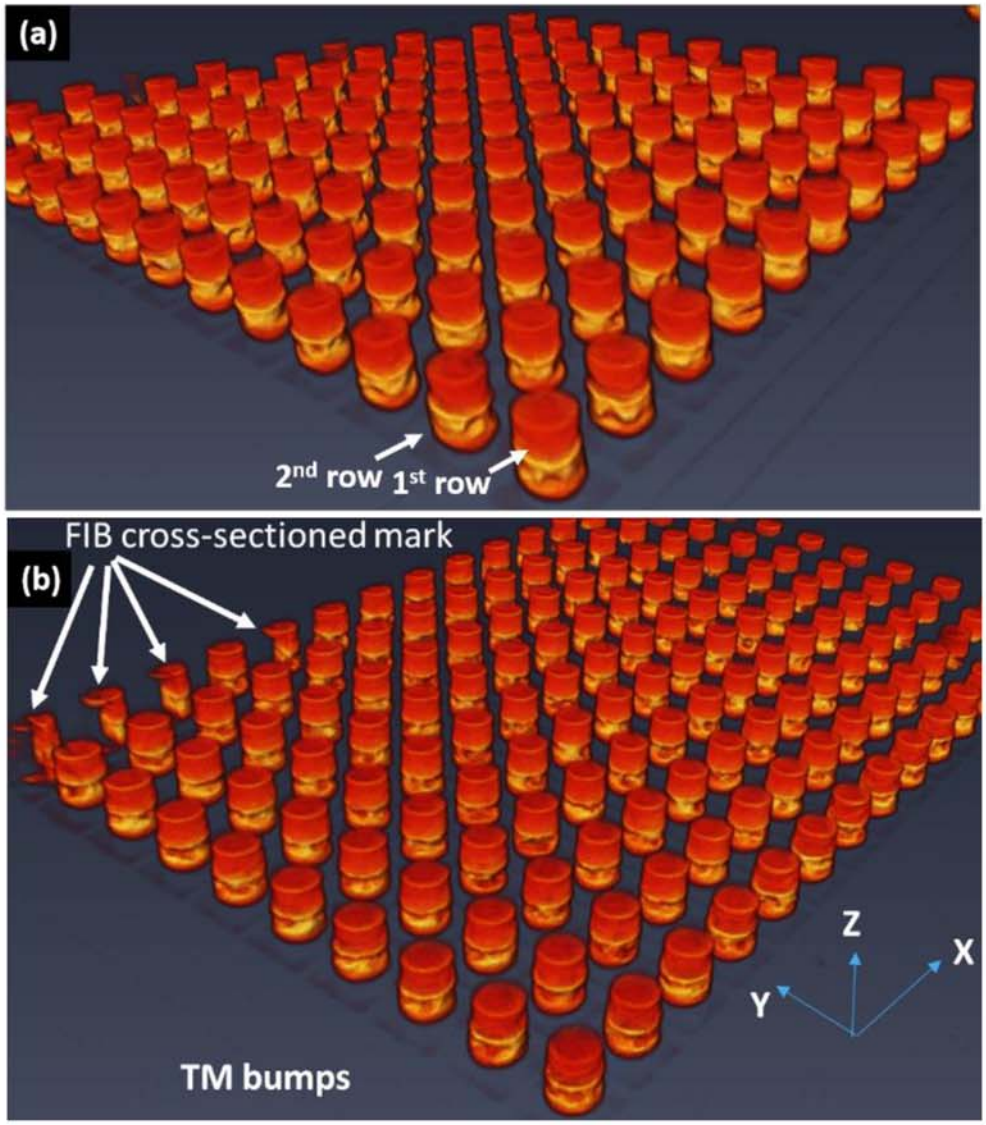

Fig. 4.12. Synchrotron Radiation X-ray micro-tomography images of (a) microbumps under Chip 2; (b) microbumps under Chip 1 after powering at 170 °C for 72 hours.

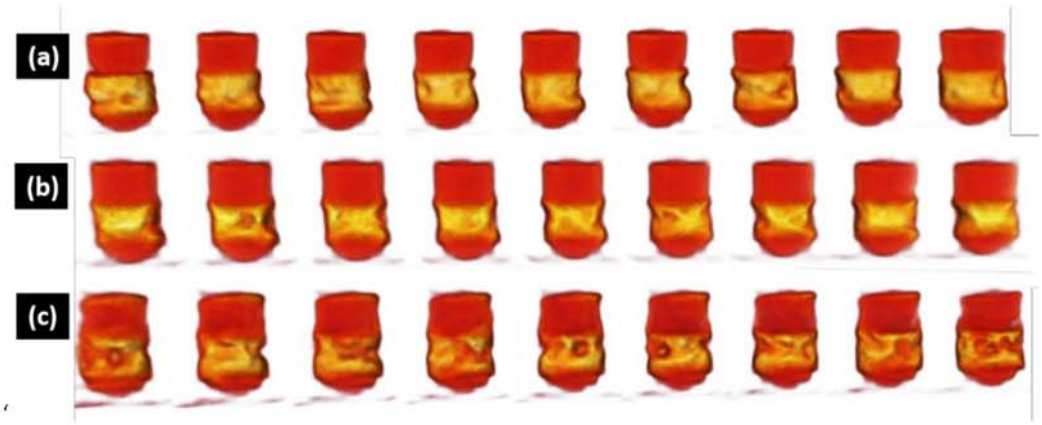

Fig. 4.13. Synchrotron Radiation X-ray micro-tomography images of a row of (a) EM bumps; (b) Annealing bumps; (c) TM bumps

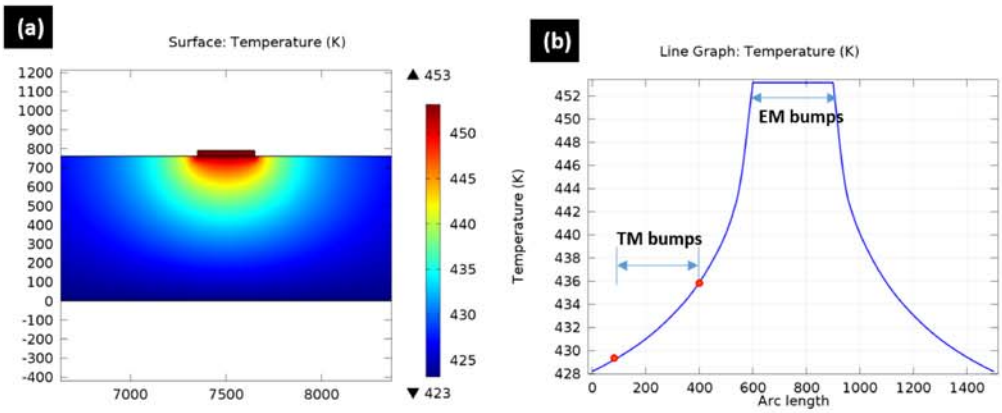

Fig. 4.14. Temperature distribution in the interposer;
(a) 2D graph; (b) 1D temperature distribution along the surface of the interposer.

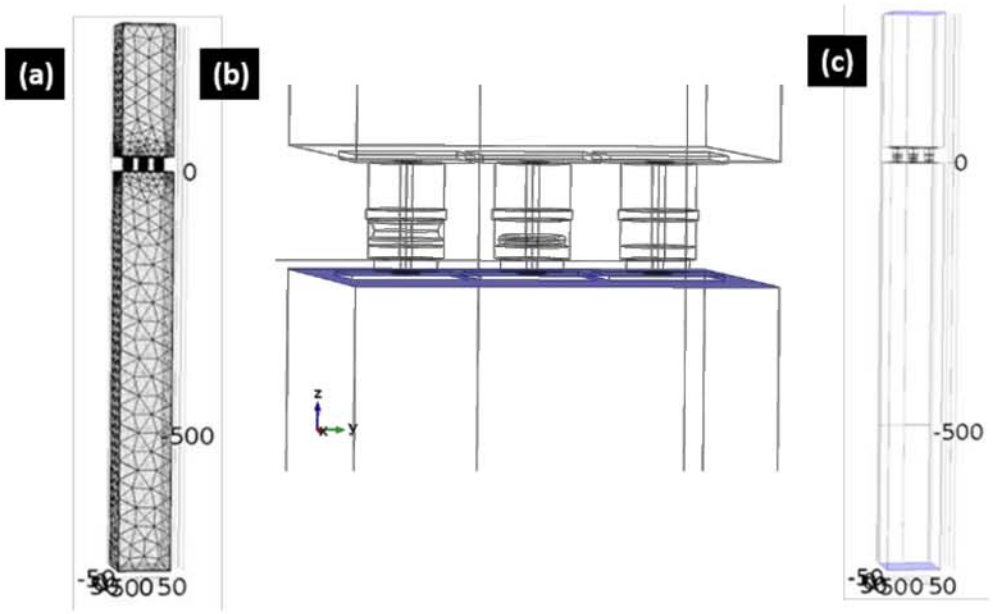

Fig. 4.15. Geometry of the simulated unit (a)3D unit; (b) Top surface of the interposer; (c) Top surface of the Si chip and the bottom surface of the interposer.

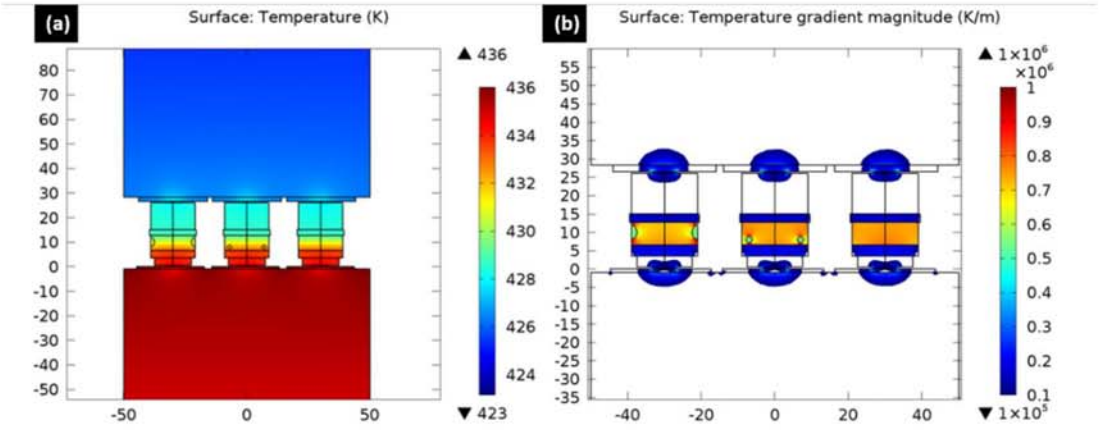

Fig. 4.16. (a) Temperature distribution; (b) Temperature gradient distribution.

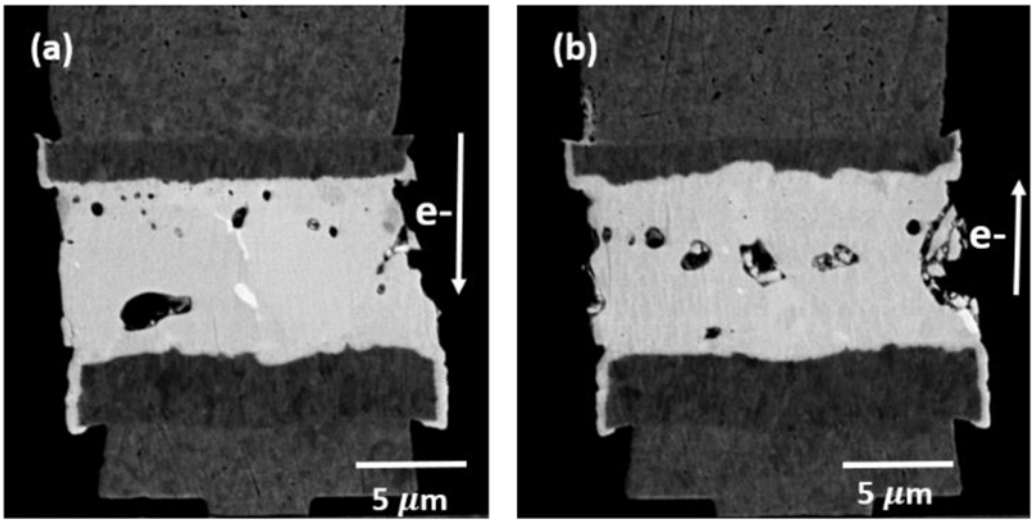

Fig. 4.17. Full IMC EM bumps that are powered after 44 hours
(a) downward EM bump; (b) upward EM bump.

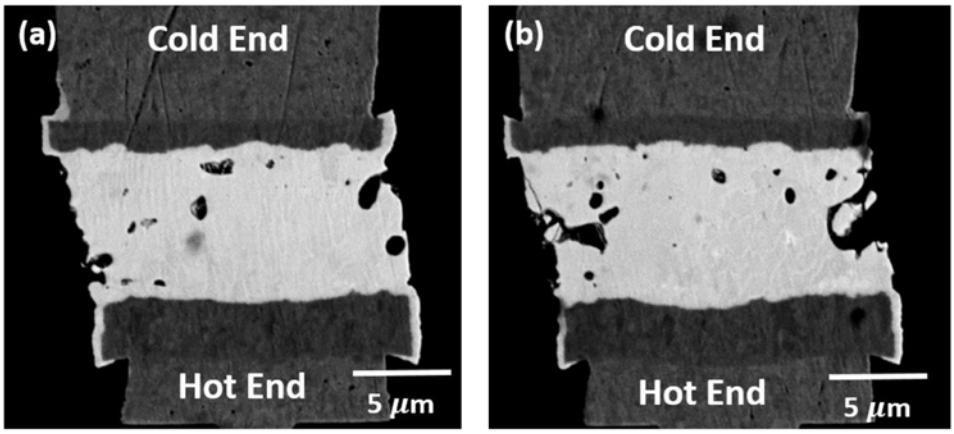

Fig. 4.18. Full IMC TM bumps after 44 hours powering.

Table 4.1. Materials Properties in the model

	Cu [14]	Al [14]	Ni [15]	Si [14]	Ni_3Sn_4 [16]	SnAg2.5 [17]
Thermal conductivity (W/m·K)	389	237	90	$150(T/300)^{-4/3}$	19.6	36.2
Heat Capacity (J/kg·K)	385	900	439	700	270	227
Density(kg/m^3)	8700	2700	8900	2329	8650	7300

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Chapter 5 Summary

Due to the scaling slow-down of Si, the advanced packaging technology is being developed to compact more functions in a small form factor. Among all of them, the stacking of Si dies vertically by 3D IC technology provides the highest packing efficiency. In 3D IC technology, the most critical issue is the increased Joule heating through denser power generation, and how does it affect the failure of the new interconnects, such as RDL, TSV, and microbumps. In this work, Joule heating induced interconnect failure through electromigration reliability test has been studied systematically.

We begin with the electromigration (EM) test of the whole 3D IC interconnect system. It is found that the increased power density in 3D IC would enhance the electromigration failure in the area where Joule heating is hard to dissipate vertically (ex. RDL in Chapter 2). The optimization of vertical heat transfer is based on reduced power density and uniformed power distribution. It is shown that connecting annular TSV all the way through super-fat RDL wire is possible to reduce Joule heating and to decrease the DC power loss. In addition, the EM resistance of fat wire RDL with cylindrical TSV is evaluated quantitatively by the SR X-ray tomography. Although the increased thickness of RDL can increase the EM lifetime, the passivation of the Cu surface at the grind side is important for robust power system.

In addition to the vertical heat transfer and its associated reliability issue, the horizontal heat transfer through Si interposer is much more neglected. The use of Si interposer in 3D IC makes the heat dissipation more efficiently, and chip package

interaction (CPI) less serious. However, the horizontal transfer between a powered die and an un-powered die through Si interposer will induce another thermal cross-talk issue. In the last section of this thesis, we evaluated the thermal-cross talk induced failure in the un-powered microbumps. It is shown that the thermal gradient in these un-powered microbumps is high enough to create thermomigration and to fail the microbumps more serious than the powered microbumps that are under electromigration. However, this is only the beginning of thermal crosstalk. It is believed that more work in the future needs to be done in order to understand the impact of thermal crosstalk, and the way to minimize its effect.