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UNIVERSITY OF CALIFORNIA

Los Angeles

Process Development and Process Window Investigation of
Copper-Silicon Dioxide Die-to-Wafer (D2W) Hybrid Bonding

A thesis submitted in partial satisfaction of the requirements
for the degree Master of Science
in Materials Science and Engineering

by

Haoxiang Ren

2021

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ABSTRACT OF THE THESIS

Process Development and Process Window Investigation of
Copper-Silicon Dioxide Die-to-Wafer (D2W) Hybrid Bonding

by

Haoxiang Ren

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2021

Professor Subramanian Srikantes Iyer, Chair

Die-to-wafer (D2W) heterogeneous integration using thermal compression bonding (TCB) faces a serious issues of Cu surface oxidation, and it is incapable of large-die assembly. Hybrid bonding, on the other hand, is considered as a candidate to replace TCB due to much better resistance to Cu oxidation and its capability for large die integration. Besides this, low temperature hybrid bonding has a great potential to achieve sub-micron pitch assembly because of a room-temperature alignment process. However, the bonding mechanism with real process issues has not yet been fully understood. In this thesis, Finite Element Analysis (FEA) and auxiliary experiments with real process issues have been implemented to explore the mechanism and the window of annealing temperature for the void-free interface. First, silicon dioxide fusion bonding is explored and optimized. A good D2W oxide bonding is achieved with 200 N of shear force (die size is 1.6 mm

$\times 1.6$ mm). The aforementioned real process issues include Cu thickness non-uniformity and real dishing conditions. A Cu thickness variation of 6.6% across the whole wafer after electroplating causes a metal dishing between 4 nm and 16 nm during chemical mechanical planarization (CMP). The critical stress (78.1 MPa) of dielectric material gives the upper boundary of temperature, and the complete contact of metal limits the lower boundary for our FEA models. The window for the annealing temperature is then simulated to be within a range between 295°C and 302°C. It is the first time that FEA with a non-uniform process input is implemented to generate a process window of D2W hybrid bonding for real world application. This thesis provides in-depth understanding and practical guidance for D2W hybrid bonding.

The thesis of Haoxiang Ren is approved.

Yu Huang

Dwight C. Streit

Subramanian Srikantes Iyer, Committee Chair

University of California, Los Angeles

2021

Dedicated to my parents and grandparents

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ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor Prof. Subramanian S. Iyer for his guidance and support in this research project. Professor Iyer's professional knowledge and enthusiastic encouragement exceedingly help me a lot, especially during the hard time of COVID-19 pandemic.

I also want to thank Professor Yu Huang and Professor Dwight C. Streit for being my master's thesis committee members. I would like to appreciate their valuable time and useful suggestions for my academic life during these two years at Dept. of MSE, UCLA.

I would like to thank my colleague and friend Yu-Tao Yang for his kind inspiration and assistance. I thank Pranav Ambhore, Dr. Zhe (Frank) Wan, Steven Moran, Ko-Ching Hou, Guangqi Ouyang, Po-Chang Shih, Arpan Dasgupta, Goutham Ezhilarasu, Niloofar Shakoorzadeh and Krutikesh Sahoo for their insightful guidance when I was naive. I also would like to extend my thanks to my lab mates: Dr. Arsalan Alam, Dr. Siva Chandra Jangam, Randall Irwin, Kannan Kalappurakal Thankappan, Ankit Kuchhang, Sepideh Nouri, Saptadeep Pal, Siyun Qiao, Golam Sabbir, Ujash Shah, and Henry Sun. They provided me with their help and suggestions generously and passionately. I especially thank Kyle Jung for his sense of humor and selfless help. I treasure all the happiness and joys that I had with my colleagues at CHIPS.

I also would like to thank my girlfriend Ziqing Han for her tolerance. Finally, I am truly and sincerely grateful to my parents Naiyan Zhang and Liming Ren, and my grandparents Linfeng Zhang and Gang Ren for their love and support. You are always the best parents and grandparents all over the world.

CHAPTER 1 INTRODUCTION

1.1 Introduction of advanced packaging technologies

Silicon technology has been developing and the device dimensions have been scaling down for several decades, following the so-called Moore's Law. More recently, the scaling has slowed down and became far more expensive. The increasing of fabrication cost (equipment, complexity, etc.) makes further scaling more difficult. Therefore, in the last decade, researcher's attention has been turned from the scaling of device dimension to the scaling of packaging. In the past, traditional packaging scaled down in moderate paces, and it was usually regarded as large form factor encapsulations because the conventional packaging is usually built on a printed circuit board (PCB), which is blocked from modern foundry techniques. Therefore, the packaging features have only scaled by 4x compared to the 1000x scaling down of the minimum chip feature[1]. Since 2015, packaging has taken off as the advanced packaging borrowed immensely from the silicon technology. This blurs the boundary of foundry and Outsourced Semiconductor Assembly and Testing (OSAT), and the packaging nowadays plays a vital role in defining system performance. With advanced packaging technologies, the inter-chip communication speed and bandwidth have been improved significantly, and the I/O pitches for interconnects have been largely reduced.

Advanced packaging usually refers to the integration of intellectual property (IP) blocks or bare dies on a single platform. There are two types of integration: homogeneous integration and heterogeneous integration.

Homogeneous (monolithic) integration is typically represented by system-on-chip (SOC). The last level of Cu wires is usually featured with fine pitches to obtain the larger data bandwidth. Also, the inter-block spacing on SOC is short, enabling smaller latency and less energy consumption. Without using diced dies, which are hard to be closely assembled, the monolithic

integration utilizes the “zero inter-die spacing” strategy to eliminates the long links between different functional blocks, compared with the traditional packaging with PCB as shown in Figure 1-1.

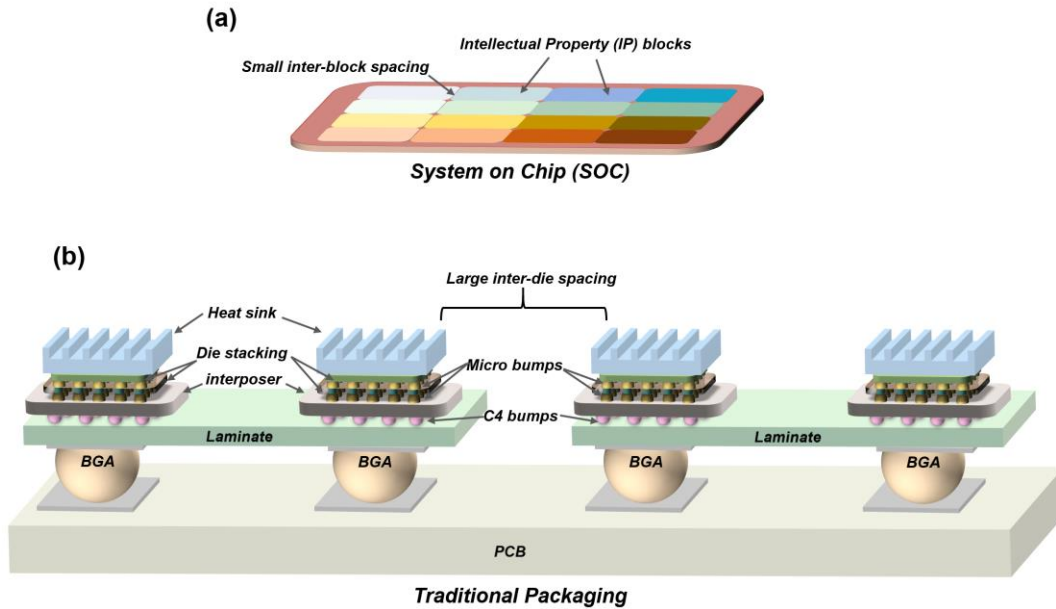


Figure 1-1: (a) System on Chip (SOC); (b) Traditional packaging

As illustrated in Figure 1-1, traditional packaging with PCB has a complex hierarchy (die, interposer, laminate, PCB) and long links to space-transform the fine pitches of last level of Cu wires on dies to the coarse trace pitches on the PCB, i.e., packaging merely fan-out Si-pitches to PCB-pitches and then fan them in again to another die/chip. Note here in Figure 1-1(b), the stacked dies are interconnected via the micro bumps (μ -bumps), which usually have 20 μm diameters and 50 μm pitches. The stacked dies are connected to the interposer also via μ -bumps. The controlled collapse chip connection (C4) bumps function as connection paths between the interposer and laminate. C4 bumps are typically around 50 μm large, with 150-500 μm pitches. The last interconnection hierarchy is the ball grid arrays (BGAs), which have about 500 μm diameters and 1 mm pitches. PCB cannot achieve fine pitches like silicon because the warpage and surface roughness on organic material precludes high-resolution lithographic patterning. Besides,

disparate materials are used in the PCB-included packaging, generating coefficient of thermal expansion (CTE)-induced thermal stress to the system. In addition, solder-based interconnects are used, involving more problems which will be discussed in the next section. Take all of these into consideration, it is necessary to eliminate the complicated packaging, and the monolithic integration is a good application of this simplification. However, there are also drawbacks to such a large system. Due to the large die size of the SOC, the fabrication yield is significantly reduced, which means manufacturing cost surges. Also, the difficulty in designing SOC largely raises the development cost and time. Furthermore, the monolithic integration leads to a homogenous system. This may limit its potential functionality a lot.

The second type of advanced packaging is heterogeneous integration. Heterogeneous integration refers to integrating dies or components from different technology nodes and disparate materials onto a single higher-level platform, enabling the improvement of functionality and performance[2]. Instead of fabricating an enormous system on a single chip/ wafer with a low yield, smaller dies obtain higher yield[3]. With the higher manufacturing yield and the assembly of known good dies (KGDs), the total cost could be reduced significantly. Furthermore, smaller dies provide less complexity and less developing time. Current heterogeneous integration includes System-in-package (SiP)[4], Chip-on-Wafer-on-Substrate (CoWoS)[5], Fan-out wafer-level packaging (FOWLP)[6], Embedded Multi-die Interconnect Bridge (EMIB)[7], and so on. These technologies successfully increased the interconnection density to some extent, but the system complexity raises the cost, and the multi-materials feature limits the scalability.

At UCLA Center for heterogeneous integration and performance scaling (CHIPS), a novel packaging platform was developed, named as Silicon-Interconnect Fabric (Si-IF)[8]. It borrows the in-expensive silicon back end of line (BEOL) technology, and achieves PCB-free, small dielets

spacing ($\leq 100 \mu\text{m}$), fine pitch ($\leq 10 \mu\text{m}$), low latency ($< 20 \text{ ps}$), and high bandwidth density (8 Tbps/mm) with an energy per bit of $< 0.15 \text{ pJ}$ [9]. With Si-IF, the electrical performance is improved significantly, and the smaller form factor and heterogeneity are obtained. In addition, the reduction of material species (only silicon, dielectric, and Cu) helps to minimize the CTE mismatch. Furthermore, the Si-IF is legacy compatible, which means the passive components and different dies with disparate pitches are allowed on this platform. Figure 1-2 illustrates the schematic of chiplets (or dielets) assembly on the Si-IF. In this thesis, the simulation is based on the Si-IF structure, and the final hybrid bonding will be built borrowing the platform of Si-IF to achieve the good performance, heterogeneity, and small formfactor.

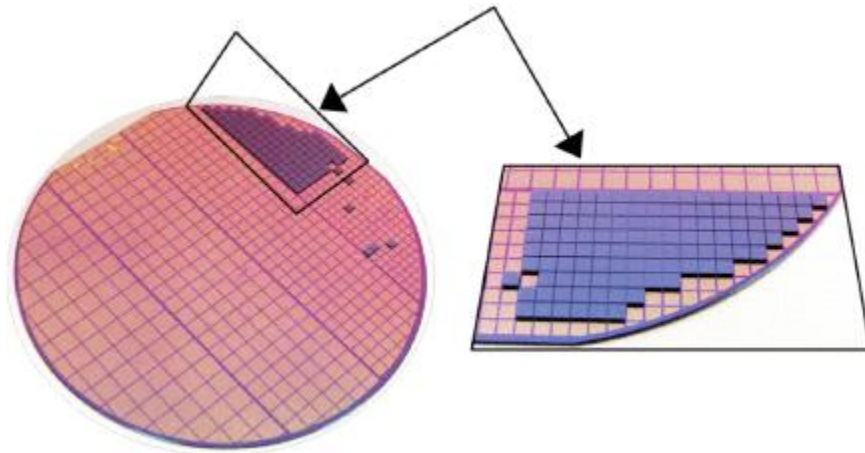


Figure 1-2 Schematic of the Si-IF, interconnect pitch is less than $10 \mu\text{m}$, and the inter-chiplet spacing is less than $100 \mu\text{m}$ [8]

1.2 Hybrid bonding and thermal compression bonding

From Rent's rule, the interconnection pitch needs to be less than $10 \mu\text{m}$ for larger bandwidth and smaller form factor at reasonable clock frequencies[10]. For most of the heterogeneous integration applications, such as three-dimensional (3D) stacking[11] in SiP, interposer technology, and Si-IF, it is hard to continuously use the solder-based bumps to achieve the high-density interconnection with fine pitch. Taking the interposer as an example, the up-to-

date interposer technology typically uses solder-based die-attach to a silicon substrate that is eventually thinned and further mounted on a laminate or PCB using coarser solder-based connections. Usually, as the packaging scales down to $\leq 50 \mu\text{m}$, solder-based bumps encounter challenges, such as solder extrusion, bridging, and intermetallic compound (IMC) formation. Therefore, the introduction of the direct Cu to Cu bonding is of immediate significance and necessity in order to eliminate the solder.

There are two approaches to obtain Cu to Cu bonding: Cu to Cu thermal compression bonding (TCB)[8], and hybrid bonding (HB)[12]. For hybrid bonding, both room temperature bonding (dielectric bonding happens first and metal bonding happens later) and simultaneous bonding for Cu-Cu and dielectric-dielectric connection are investigated. However, the room temperature hybrid bonding is more attractive and more extensively studied due to its higher throughput than the latter one. Though TCB can scale to about $6 \mu\text{m}$ pitch, room temperature hybrid bonding overcomes some issues which TCB meets with. The comparison of TCB and room temperature HB is outlined in Table 1-1 below (the advantage of room temperature HB is colored as green, and the disadvantages of room temperature HB is colored as red):

Table 1-1 Comparison of TCB and room temperature HB

TCB		HB
Pressure for metal–metal bonding	External pressure from machine motor	Internal pressure from metal thermal expansion; independent of die size
Encapsulation and passivation	Passivation required	Encapsulation is naturally formed; Cu diffusion issue due to misalignment
Throughput	Low	High
Alignment	Thermal gradients make accurate alignment difficult	Room temperature tacking makes alignment more accurate
Particulate sensitivity	Low	High
Planarity	More tolerant	Metal recess depth is critical; critical dielectric roughness is required

Thermal compression bonding has been demonstrated[8] to have the interconnection pitch below 10 μm for robust and reliable heterogeneous integration application. Nonetheless, challenges in TCB still exist: (1) TCB is challenging to be implemented on large dies since the external TCB force on commercial assembly tools is limited. Furthermore, as the areal bond density increases, the pressure on each bond decreases proportionally. (2) Additionally, the metal surfaces are susceptible to oxidation at typical bonding temperatures as the TCB process is conducted in air. So a special surface passivation layer is required on the top of metal films[13]–[16]. Also, during device operation, encapsulation is needed around the metal[17], [18]. (3) The throughput of TCB is modest for die-to-wafer (D2W) bonding because of the time needed for temperatures to ramp up and down. (4) Finally, since the temperature of the alignment and bonding process is high, the thermal expansion in optics degrades the alignment and overlay, preventing interconnection pitch from scaling down to finer pitch.

Hybrid bonding as shown in Figure 1-3, on the other hand, is capable of minimizing these drawbacks of TCB. (1) The essence of hybrid bonding is hydrostatic pressure generated internally. This self-generated pressure is induced by the differential coefficient of thermal expansion (CTE) of metal over the confining dielectric material, which means that the pressure is independent of the die size and can be applied to large dies. (2) Since the preliminary tacking step (tacking refers to the initial Van der Waals bond of the two mating dielectric layers usually silicon dioxide) happens near room temperature, metal oxidation is minimized. The surface passivation layer while preferred is no longer critical. Furthermore, the surrounding dielectric material can encapsulate metal film naturally during the tacking step at room temperature. This can isolate metal films from environmental oxygen during the annealing step and the operation. (3) For each die, the tacking time is few seconds compared to several seconds per die in TCB. In the batch annealing process,

hundreds of dies can be annealed together. Therefore, the throughput in hybrid bonding can be significantly increased. (4) With the tacking of dielectric at room temperature, the alignment overlay can be improved due to the absence of thermal gradient in optics. This can potentially drive the assembly to a finer pitch.

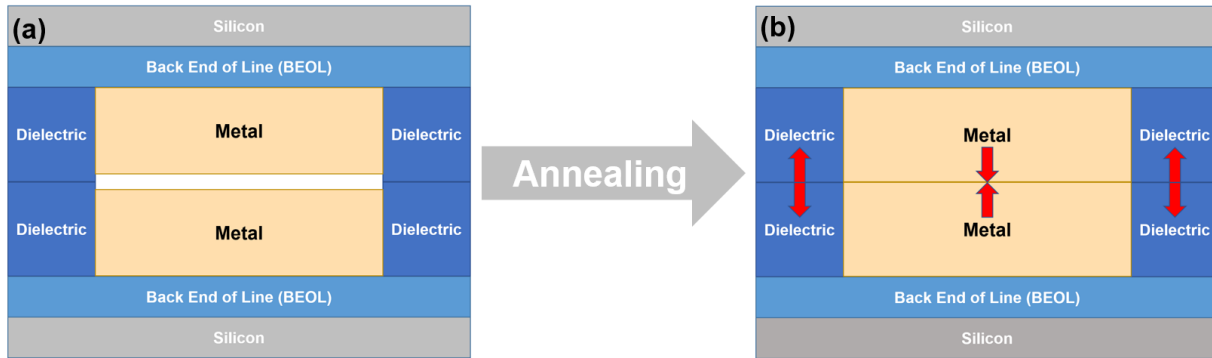


Figure 1-3 Schematic of hybrid bonding: (a) Dielectric to dielectric initially bond at room temperature; (b) Heating bridges the dishing gap and enables metal to metal bonding without external pressure (metal CTE > dielectric CTE)

1.3 Objective of this work

Although hybrid bonding has been applied extensively to wafer-to-wafer (W2W) bonding[19]–[21], especially in the field of CMOS image sensors (CIS)[22], [23], the detailed thermo-mechanics has not been comprehensively studied. In this thesis, we focus on D2W hybrid bonding for two reasons: heterogeneous integration via dielets or chiplets is catching attraction in the implementation of high-performance systems; and at the individual contact level, there is no significant difference between die-to-die, die-to-wafer or for that matter wafer-to-wafer hybrid bonding.

In the past few years, multiple studies of hybrid bonding have been discussed with the perspective of analytical modeling[24] and Finite Element Analysis (FEA) simulations[25]–[29]. Here, we further explore the key process parameters and the window of D2W hybrid bonding. This work aims to study basic fusion bonding and hybrid bonding, and explore the effect of non-

uniformity on the process window of hybrid bonding using FEA modeling. The main contributions are as follows:

- 1) Developing and optimizing the fusion bonding, including thermally grown silicon dioxide bonding and the plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide bonding.

- 2) Conducting the parametric investigations on D2W hybrid bonding. Establishing the FEA model to set up the process window with respect to temperature and dishing depth for void-free and robust D2W hybrid bonding by studying the internal stress on metal vias/pads and the peeling stress on dielectric bonding interfaces. The effect of the non-uniformity of metal electroplating on dishing depth variation is also studied, and a more accurate and narrow process window is thus obtained to give a better understanding of D2W hybrid bonding.

1.4 Organization of this thesis

In this thesis, we introduced the subject of advanced packaging and hybrid bonding in Chapter 1. Fusion bonding optimization is discussed in Chapter 2. Next, in Chapter 3, the process window of D2W hybrid bonding is investigated. In Chapter 4, the conclusion is summarized along with the future work.

CHAPTER 2 LOW TEMPERATURE DIELECTRIC BONDING

2.1 Introduction of fusion bonding

Fusion bonding usually refers to the direct bonding of nearly any kind of material, which forms interface at microscopically close distance and then adhere through van der Waals attraction forces under room temperature. The two contacting surfaces should be flat and clean enough to meet the requirement of “microscopically close”. Details of the influence of the global non-uniformity and local roughness on the bonding strength will be discussed later. Fusion bonding is also known as direct bonding, or more informally regarded as gluing without glue[30].

Fusion bonding was first discovered in metal bonding. Desaguliers reported that if a lead surface is touch-polished and pressed together to get close enough, the two lead pieces would be bonded[31]. Fusion bonding for metal (relatively soft material) is based on the plastic deformation to achieve the close contact of atoms and the following bonding. Note the metal fusion bonding here is not the same as thermal compression bonding (TCB) which is a diffusion-based bonding. It is difficult for brittle materials to obtain the plastic deformation, but people still found that hard materials such as silica or silicon could be bonded if the surfaces are flat and clean enough[32]–[35]. The attraction force is attributed to the hydrogen bonds between two mated surfaces[30]. The strength of the hydrogen bonds is large enough to elastically deform the brittle materials, overcoming the warpage and the waviness (spatial wavelength of the order of 0.1-1 mm)[36] over the entire surface of the bulk materials during room temperature contacting. Besides the global warpage or bowing, and the “semi-global” waviness, the local roughness (in the range of nanometers or angstroms) also plays a vital role in the direct bonding. It is believed that only the surfaces with low roughness could be bonded firmly under room temperature. With more in-depth studies in the field of fusion bonding, one of its most significant applications—silicon on insulator

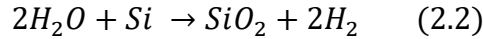
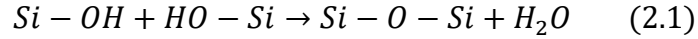
(SOI) has proliferated. Initially, the Separation by Implantation of Oxygen (SIMOX) was used to form the buried oxide layer (BOX), but the defects generated by the ion implantation render the quality of top silicon layer to be largely unsatisfied for device fabrication, and also the cost is relatively high. With the developing of fusion bonding, the bond and grind back SOI (BGSOI)[37], bond and etch back SOI (BESOI)[33], and the SmartCuttm[38] have emerged to replace the SIMOX completely.

Though fusion bonding is referred as “room temperature bonding”, the van der Waals forces and the hydrogen bonds are not sufficient to be treated as a permanent bond. After the low temperature tacking, high temperature annealing is also needed to transform the temporary weak bonds into the strong permanent bonds. Consider the silicon wafer bonding as an example, the bonding mechanism and process is discussed below[30], [39]:

1. Two well-polished and ultra-clean silicon dioxide surfaces (usually and the proven best case is native oxide to thermal oxide) are prepared and brought into close contact in air and at room temperature. The surfaces may be plasma treated, and are terminated with the polar hydroxyl group. The two surfaces are hydrophilic in both cases with and without plasma treatment. Due to the van der Waals type hydrogen bonds, the two wafers are physically bonded. The environment should be a high-quality cleanroom (class 10 or better) or a specific bonding tool with clean (frequently vacuum) chamber. Note that the two surfaces are naturally covered with several monolayers of water molecules since the wafers are prepared in ambient atmosphere, and these water molecules help with the hydrogen bonding during the first step.

2. Low temperature heating follows to facilitate the chemical reaction. At about 100°C (it could happen either during ramp up, or during dwelling time and temperature) for the no-plasma scenario (or at room temperature for plasma-treated scenario), the initially existing or reaction-

generated water molecules could diffuse vertically through the silicon dioxide to oxidize the silicon underneath, or diffuse along with the bonding interface to the edge of the wafers. The reaction to generate water molecules and the reaction to oxidize the silicon are below:



As can be seen, both reactions generate a non-solid product. Water molecules generated in equation (2.1) prefer a thinner oxide layer to pass through and then react with silicon. From this perspective, the native oxide is favored since it has a shorter path for the water molecules to travel. According to the equation (2.2), when the silicon was oxidized, hydrogen molecules are formed and the pressure would increase in between the interface[40]. This might cause the formation of hydrogen gas bubbles at the bonding interface, which is harmful to robust bonding[41].

3. high temperature annealing for the stronger covalent bonds. The temperature is typically higher than 800°C without plasma and around 200°C with the plasma treatment[39]. During this step, for the no-plasma situation, the silicon dioxide starts to soften and deform, and the viscous flow enables bonding interface to overcome the local roughness and be close to each other at the atomic level[36]. For the plasma-treated situation, since one of the wafers is a silicon wafer with thin native oxide, the oxidation of the Si bulk is responsible for the closing of the interfacial gaps[39]. Note here that the plasma treatment generates water reservoir (by bombardment) for later Si oxidation during annealing. Also, the generated hydrogen gas during the process described by equation (2.2) begins to diffuse through the silicon dioxide layer, thus the formation of bubbles is hindered. From this perspective, the thicker the thermal oxide layer, the better for the reliable bonding. Consider all of the water molecules reduction, oxidation of the plasma enhanced bonding

samples, and hydrogen degassing, the best combination of wafer bonding for SOI is Si with native oxide to relatively thick thermal oxide.

Though the dielectric fusion bonding has been explored in detail for example in the fabrication of SOI wafers, these are limited in the bonding of blanket virgin Si wafers with native oxide to the Si wafer with high quality and atomically smooth thermal oxide as mentioned above. For hybrid bonding application, thick, multi-layer dielectrics (typically named as the inter-level dielectric (ILD)) are necessary for the metal wiring during the process of back end of line (BEOL). The oxides are deposited usually by PECVD and the surface is patterned. Both these are expected to degrade the bond. In this thesis, thick thermal oxide and plasma enhanced chemical vapor deposition (PECVD) oxide were used for the bonding experiment instead of bulk silicon with native oxide or thin thermal oxide. The detailed experiment process and results will be discussed in the next section.

2.2 Experiment and results

2.2.1 Thermal oxide bonding

2.2.1.1 overview

Thermal oxidation has been chosen to be the best method to get the high-quality dielectric film with the lowest interface trap densities, compared with the deposited film, plasma reaction oxidized film, and electrochemical anodized film[42]. For both dry oxide and wet oxide formation, the temperature in the furnace is supposed to be around 900°C to 1200°C. The gas flow and temperature ramping are delicately controlled by a microprocessor to minimize the non-uniformity and wafer warpage. In this work, both dry thermal oxide and wet thermal oxide are explored. The non-uniformity and the roughness for wet oxide are listed below in the Table

2-1. These properties of dry oxide (not listed in this thesis) are close to or even better than those of wet oxide.

Table 2-1 Uniformity and surface roughness of wet thermal oxide

Properties	Values
Non-uniformity (\AA)	100-200
Surface roughness (RMS) (\AA)	<5

The non-uniformity was detected by NanoSpec reflectometer. The thickness was calculated by the microprocessor in the reflectometer using the interfered reflections pattern. Measurement was conducted from the center to the edge across the 4-inch wafer. 9 points are tested on each wafer, and each point is measured 3 times. The lowest points are usually located at the center, and the highest points are typically at the edge. The definition of non-uniformity here is the maximum thickness (highness point) minus the minimum thickness (lowest point).

The surface roughness was characterized by Bruker Dimension FastScan Scanning Probe Microscope (SPM). Peak-force tapping mode was employed with 2 kHz peak force frequency. Root mean square (RMS) roughness data was obtained via the height sensor channel, and the scan size is $1\ \mu\text{m} \times 1\ \mu\text{m}$.

As can be seen, thermal oxide has excellent surface conditions. Thus, before any bonding of PECVD oxide was conducted, thermal oxide was first tried (to mimic the good PECVD oxide film) for the bonding test experiment. Both wafer-to-wafer (W2W) bonding and die-to-wafer (D2W) bonding were done in this work. For D2W bonding, in reality, the die-to-substrate bonding was conducted to mimic the D2W bonding. At the individual contact level, there is no significant difference between die-to-substrate and die-to-wafer bonding. The W2W bonding process is relatively simple: prepare two Si wafers with thermal oxide on top and clean the wafers (the clean process will be discussed in detail in D2W process); apply Ar/H₂ plasma treatment on the two

surfaces; and then manually align the two wafers, and hit the center of the bonded wafers to initialize the bonding wave (squeeze the air out). The wafers pair is then be sent into a 200°C vacuum oven to enhance the bonding. The bonding results are shown in 2.2.1.3 section.

2.2.1.2 fabrication flow of die-to-wafer (D2W) testing unit

With the good performance shown in Table 2-1, thermal oxide was fabricated and bonded. The process flow is shown below in Figure 2-1.

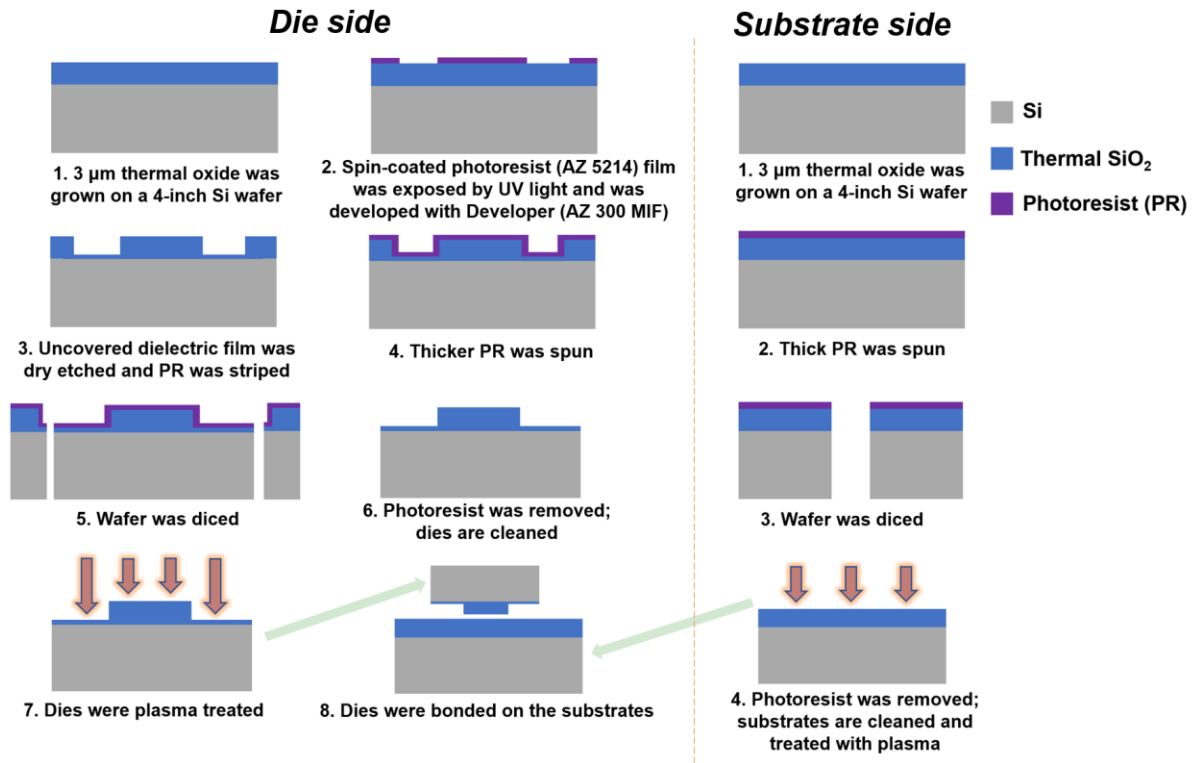


Figure 2-1 Process flow of thermal oxide bonding experiment

Pre-Furnace Clean (PFC) and thermal oxidation: since the surface condition of the as-received wafer is not ideal for getting a flat and uniform thermal oxide layer, pre-furnace clean is necessary and important. The first step is the Piranha clean (mixture of sulfuric acid, hydrogen peroxide, and water), which gets rid of all organic and metallic contaminants. Following is the HF clean which removes the native oxide layer on the silicon. The cleaned wafers are then be water

rinsed and spin dried. As long as the wafers are clean and dry (no water drops on the surface), they are put into the 1100°C furnaces in a wet environment for around 30 hours and 3 μm of thermal oxide is obtained.

Mesa patterning: during the singulation process, the edge of the diced dies (or chips) is usually chipped, deformed, and dirty, which affects the bonding strength significantly. Chipping of the die edge after dicing is shown in Figure 2-2. Therefore, the protruded mesa structure is needed to avoid the contact of the die edge during the oxide bonding process.

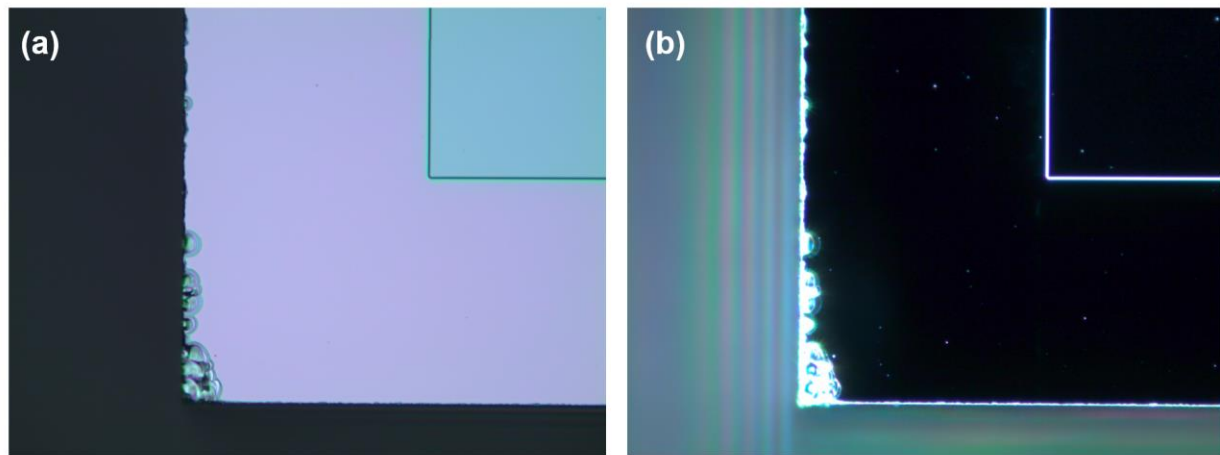


Figure 2-2 Chipping at the die corner after dicing: (a) Bright field; (b) Dark field

We pattern the mesa lithographically. Before any photoresist is spun on the wafer surface, pre-spin coating clean is necessary. The wafer is rinsed with acetone, methanol, isopropanol (IPA) and de-ionized (DI) water. Note that during the fabrication process, each cleaning step is mandatory and important. Any particles or defects might significantly lower the yield, influence the system performance, or even sometimes fail the process, especially in hybrid bonding. Acetone is for removing the organic contaminants. It is a good polar solvent which can dissolve most of the organic particles. Methanol is used to eliminate the remaining organic particles that have not been removed by acetone. IPA is a non-polar solvent to remove the non-polar organic residue and the acetone/ methanol solvent containing organic particles. DI water is used to wash out the residues

and any organic solvents thoroughly. After cleaning, the wafer is dried with nitrogen gas and put on the hotplate for about 2 minutes. Once the wafer is dehydrated, it is kept inside the Bis(trimethylsilyl)amine (HMDS) tank to promote the adhesion of photoresist (PR) to the wafer. Then the wafer is put on the spin coater and poured with positive PR AZ 5214. The main spinning speed is 2000 rpm, and the deposited PR film thickness is about 2 μm . The PR is then soft baked and exposed with $80\text{mJ}/\text{cm}^2$ energy from 365 nm wavelength mercury bulb. The exposed PR is then developed with AZ 300 MIF developer and hard baked.

Etching: the silicon dioxide film is then etched with CHF_3 , C_4F_8 and Ar plasma. The mesa part is protected with the 2 μm PR, and the selectivity of PR/ SiO_2 in such an etching environment is about 1:3. The non-protected part is etched off 2.5 μm , and the PR was stripped with O_2 plasma at 250°C . The D2W hybrid bonding is susceptible to particle contamination, i.e., D2W hybrid bonding is prone to generate contaminants during the singulation process, and this is a huge detractor of yield. Coating of protective layer during the dirty saw dicing process is studied for higher yield[43], [44]. Thus, the mesa structure is subsequently spun with 4 μm of PR as the protective layer for saw dicing to avoid contamination.

Singulation: the wafer is diced with a diamond blade. Two wafers are diced in this step, one is for dies (upper part for bonding), another is for substrate (lower part for bonding). The die size is $2.1\text{ mm} \times 2.1\text{ mm}$, and the substrate size is $6\text{ mm} \times 20\text{ mm}$. Note that the mesa structure is only on the dies.

Cleaning and surface treatment: the protective PR is striped off and the dies/ substrates are cleaned thoroughly and then inspected carefully. The cleanness of the pre-bonding sample is of vital importance. Even one single particle is able to reduce the bonding strength significantly. The cleaned die is pictured below in Figure 2-3. Figure 2-3 (a) and (b) show the clean sample, and

Figure 2-3 (c) and (d) show the sample with insufficient cleaning. In the dirty one, every particle, bubble, or defect would affect the bonding. The cleaned samples are treated with different source of plasma. O₂ plasma, Ar plasma, and Ar/H₂ plasma were used, and the influence of plasma treatment on the bonding strength will be shown later.

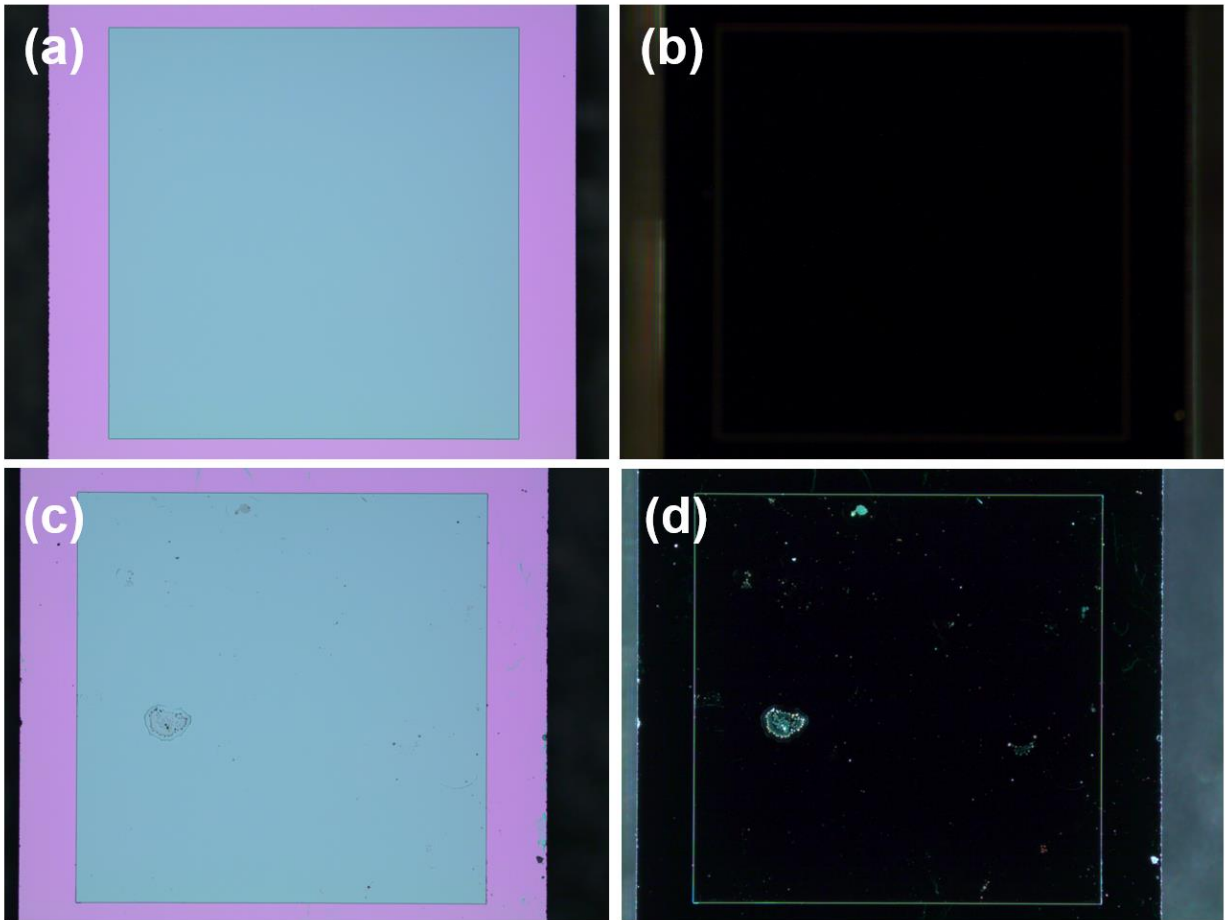


Figure 2-3 (a) Bright field image of clean sample; (b) Dark field image of clean sample; (c) Bright field image of dirty sample; (d) Dark field image of dirty sample

Bonding: The dies/ substrates are then bonded by a modified die to wafer bonder from Kulicke & Soffa (K&S), which is shown in Figure 2-4. Different parameters are listed below. After the low temperature tacking, the temporarily bonded die-substrate pairs are put into an oven. For this step where Cu is not involved, convection oven is fine. However, later when hybrid bonding

is performed, vacuum oven is needed. Also, parameters for high-temperature annealing are listed in Table 2-2.



Figure 2-4 Die to wafer bonder from K&S

Table 2-2 Parameters for oxide tacking and annealing

Conditions	Parameters
Tacking temperature	35°C, 60°C, 120°C, 180°C, 210°C, 240°C
Tacking force	1 N, 5 N, 20 N, 50 N, 100 N, 150 N, 200 N, 250 N, 300 N
Main tacking duration	0.5 s, 1.5 s, 10 s
Annealing temperature	100°C, 150°C, 200°C, 250°C, 300°C
Annealing duration	1 hr, 2 hr

2.2.1.3 bonding results and discussions

The bonded die-substrate pairs were tested by the shear force testing tool as shown in Figure 2-5.



Figure 2-5 Dage tool to shear dies from the substrate

With all the parameters listed in Table 2-2, the shear force testing results are shown in Figure 2-6. Note here that the Ar/ H₂ plasma treatment was performed for these samples.

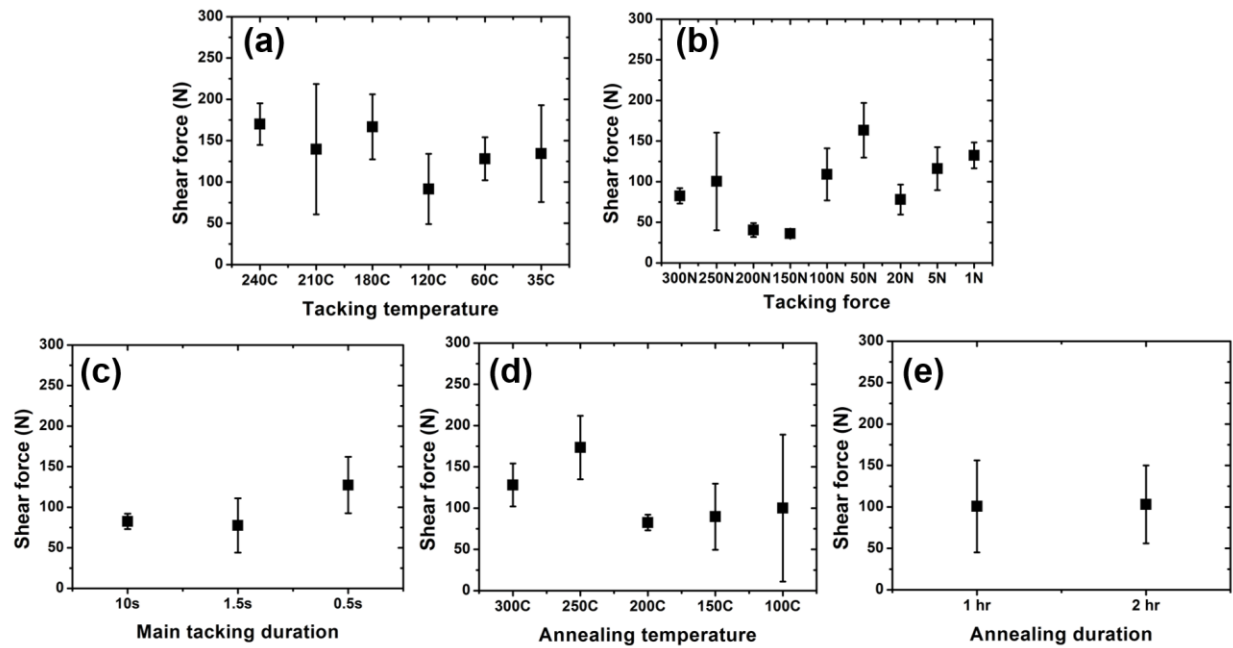


Figure 2-6 (a) Shear force vs. tacking temperature; (b) Shear force vs. tacking force; (c) Shear force vs. main tacking duration; (d) Shear force vs. annealing temperature; (e) Shear force vs. annealing duration

Since the low temperature hybrid bonding is the final goal, and the bonding strength at 35°C shows satisfactory results, the tacking temperature of 35°C is chosen. From Figure 2-6(b), the tacking force of 50 N yields the strongest bonds. The tacking force should not be too small, since it initiates the bonding wave even though the die size is small and helps dies to overcome the warpage. Also, the tacking force should not be too large, and the two hypotheses we made are: large force might cause micro-cracks and thus damage the dies; or the die is adhered on the placer (die holder on the bonder during the bonding process) after the bonding which weakens the bonding in reality (imagine the placer pulls the die up from the substrate). From Figure 2-6(c), the main tacking duration doesn't affect the bonding results notably; therefore the 0.5 second is chosen due to it gains the relatively high shear force.

For the annealing conditions, though the 250°C temperature helps to get stronger bonds, that temperature might be too high for hybrid bonding. At this step, 200°C annealing temperature is selected, and the reasons would be discussed in detail in the next chapter. Also, since the annealing duration does not affect the bonding strength considerably, 1-hour duration is chosen for higher throughput.

Then, different types of surface treatment will be discussed. The optimized tacking and annealing parameters (35°C tacking temperature, 50 N tacking force, 0.5 s main tacking duration, 200°C annealing temperature, 1 hour annealing duration) are employed. Theoretically, O₂ plasma treatment would result in more hydrophilic surfaces. However, achieving hybrid bonding with Cu exposed on the surfaces is our final goal, and the oxygen obviously would oxidize the metal. We used both O₂ plasma and Ar plasma to compare the influence of hydrophilicity on bonding strength, and we also tried Ar/ H₂ plasma since it might be the potential treatment method for hybrid bonding (it is a good treatment for Cu-Cu thermal compression bonding). H₂ is the reducing agent that

prevents the oxidation of Cu, and Ar is to clean the mating surfaces via the surface activated bonding (SAB) process. The shear force testing results are shown below in Figure 2-7 (a). The scanning electron microscope (SEM) cross section image of Ar/H₂ plasma treated bonded samples is shown in Figure 2-7 (b), which indicates good dielectric bonding (the defects at interface may be generated during polishing of sample which is in the resin for imaging the cross section).

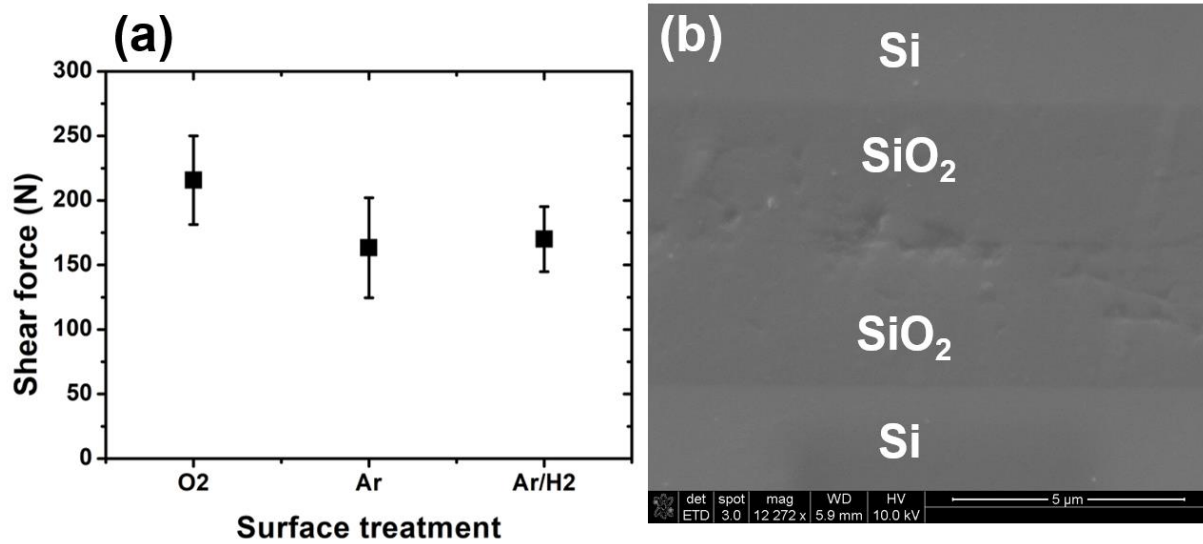


Figure 2-7 (a) Shear force vs. surface treatment; (b) SEM cross section image of bonded thermal oxide

The testing results demonstrate that the Ar plasma treatment and Ar/ H₂ plasma treatment would not affect the bonding drastically, so the Ar/ H₂ plasma treatment is selected due to its reducing property.

For W2W bonding, we did not use the Maszara's crack opening method (blade insertion) or pull test to test the bonding strength, but only manually shear the bonded wafers to get a rough understanding of the bonding strength. The wafer-to-wafer bonding with thermal oxide is strong enough to overcome the maximum force that a graduate student could apply. So far, we haven't plan to do hybrid bonding in three-dimension (3D) stacking application (for 3D stacking, the bonds need to be strong enough to guarantee that dies could withstand the force originated from the

thinning process), and our final goal is to achieve D2W hybrid bonding (we conduct W2W bonding to complete the design of experiment and explore the potential W2W hybrid bonding application). Therefore, this W2W bonding results with manual testing is good enough. Blade insertion or pull test would be conducted in the future.

2.2.2 PECVD oxide

2.2.2.1 overview

Though we have got good bonding results of the thermal oxide, our final goal is to build the die-to-wafer hybrid bonding, and on both die side and wafer side, multi-layer of metal-dielectric is required for wiring. Deposited dielectric is typically employed, and PECVD is a good candidate due to its relatively low temperature and high film quality and uniformity.

At UCLA Nanolab, STS Multiplex PECVD is the tool for silicon dioxide deposition. During depositing, the platen temperature is kept at 300°C, and the process pressure is 900 mTorr. N₂, N₂O, SiH₄ are ionized to form plasma by a 30-Watt high frequency (HF) power showerhead. The deposition rate is about 50 nm/min.

The non-uniformity from center to edge of the 4-inch wafer with 3 μm PECVD oxide, and the RMS roughness are listed below in Table 2-3. As mentioned above, for die-to-die, die-to-wafer, or wafer-to-wafer hybrid bonding/ oxide bonding, the surface roughness impacts the effective contact area and diminishes the bonding strength. Researchers always tried to get lower roughness[45], [46]. For die-to-wafer or wafer-to-wafer bonding, not only the surface roughness, but the non-uniformity as well directly and indirectly affects the bonding strength. The “direct perspective” is that the wafers are either partially bonded or overcome the non-uniformity by warping during the tacking process. The “indirect perspective” is that the non-uniformity will build

up during the later Cu electroplating, chemical-mechanical polishing (CMP), and dielectric dry etching process. This effect is under investigation now and not included in this thesis. Therefore, getting as-low-as-possible surface roughness and non-uniformity is critically high-ranking for the good bonding.

Table 2-3 Uniformity and surface roughness of 3 μm PECVD oxide (as deposited)

Properties	Values
Non-uniformity (\AA)	700-1200
Surface roughness (RMS) (\AA)	50-90

2.2.2.2 characterization, bonding results, and discussion

According to Table 2-3, both of non-uniformity and surface roughness are not tolerable for reliable bonding. Several methods are utilized in this work to minimize the non-uniformity and roughness. These methods include high-temperature densification, CMP, and plasma treatment.

For non-uniformity, the maximum thickness from center to the edge of the wafer is measured with respect to the total thickness of the deposited silicon dioxide layer. The results are shown in Table 2-4.

Table 2-4 Non-uniformity vs. PECVD oxide thickness

Thickness (nm)	Non-uniformity (\AA)
127	19
320	115
691	198
3000	400-1500

According to Table 2-4, with the thickness goes up, the non-uniformity also increases.

For surface roughness, the oxide thickness- roughness map was obtained first. All the PECVD oxide was deposited on top of a 500 nm thick thermal oxide (pad oxide). 127 nm (5 minutes deposition in STS PECVD), 320 nm (10 minutes), 690 nm (20 minutes), and 3 μm of

oxide were deposited, and the roughness was measured. The roughness results are shown below in Figure 2-8.

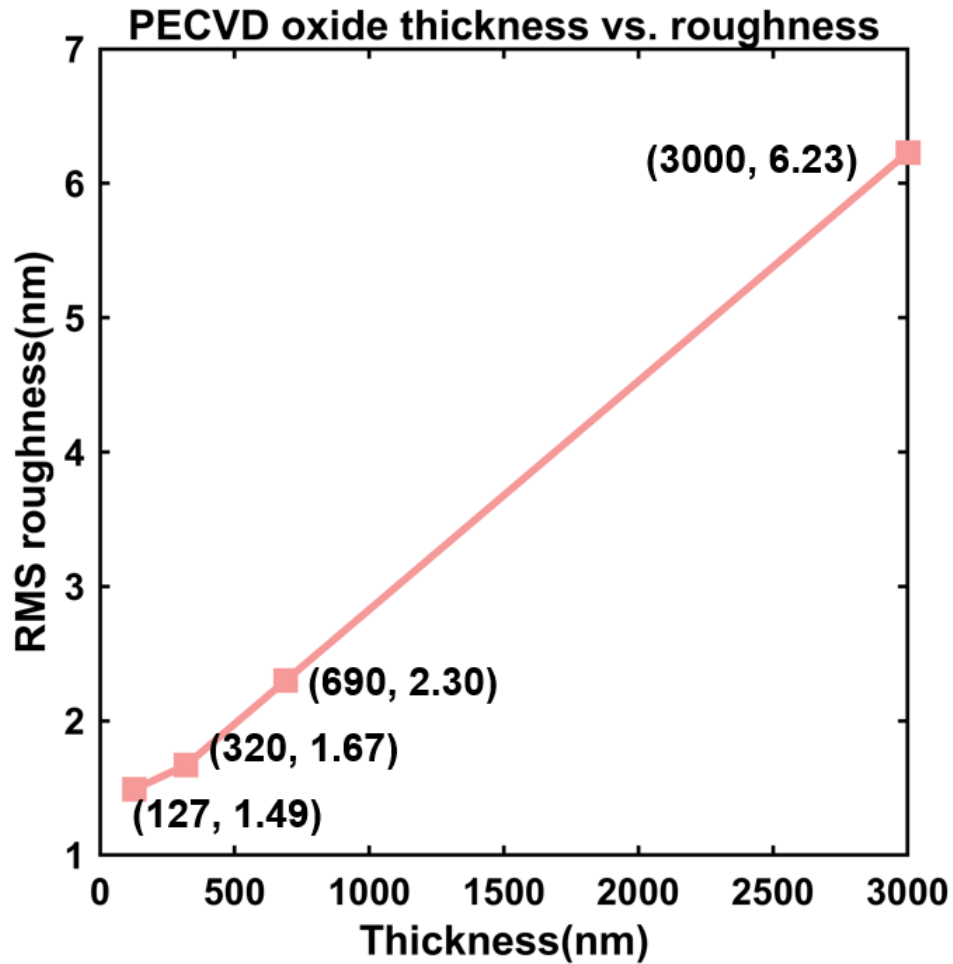


Figure 2-8 PECVD oxide thickness vs. root mean square (RMS) roughness

As can be seen, as the thickness grows, the surface roughness gets worse. Based on this, densification and plasma treatments were performed on wafers with different thicknesses of PECVD oxide. The results are listed below in Table 2-5.

Table 2-5 Surface roughness and non-uniformity results

oxide source	thickness (nm)	plasma treatment	densification at 360°C for 16 hours	touch polish with H ₂ O for 120 s	average RMS roughness (nm)	non-uniformity across the wafer (Å)
PECVD	127 (5 min)	no	no	no	1.49	19
		Ar 30s	no	no	0.65	-
		Ar 90s	no	no	0.38	-
		Ar + N ₂ 90 s	no	no	0.50	-
		Ar + H ₂ 90 s	no	no	0.46	-
	320 (10 min)	no	no	no	1.67	115
		no	yes	yes	1.49	93
	691 (20 min)	no	no	no	2.30	188
		no	yes	yes	2.26	163
		Ar + N ₂ 90 s	no	no	1.10	160
		Ar + N ₂ 90 s	yes	yes	1.10	133
	3000	no	no	no	6.02	1463
		no	yes	no	2.36	1076
		no	yes	yes	2.48	935
		Ar (80W) 90 s	yes	no	2.34	611
		Ar (150W) 90 s	yes	no	2.09	1138
		Ar +H ₂ 90 s	yes	yes	2.31	901
wet thermal	3000	no	no	no	0.22	100

Usually, the densification occurs at relatively high temperature for long duration, degassing and reducing the defects (lessening the gas reservoir). We also take advantage of the lucky side effect of lowering surface roughness after densification in this work. For CMP, more work still needs to be done. Both water polishing and silica slurry polishing are tried, but the ideal roughness is not obtained. Different plasma treatments have similar effect, which is re-deposition of the atoms on

the surface. The AFM comparison of before and after plasma treatment for 90 seconds in argon/nitrogen at 75 Watt of power treatment is shown in Figure 2-9.

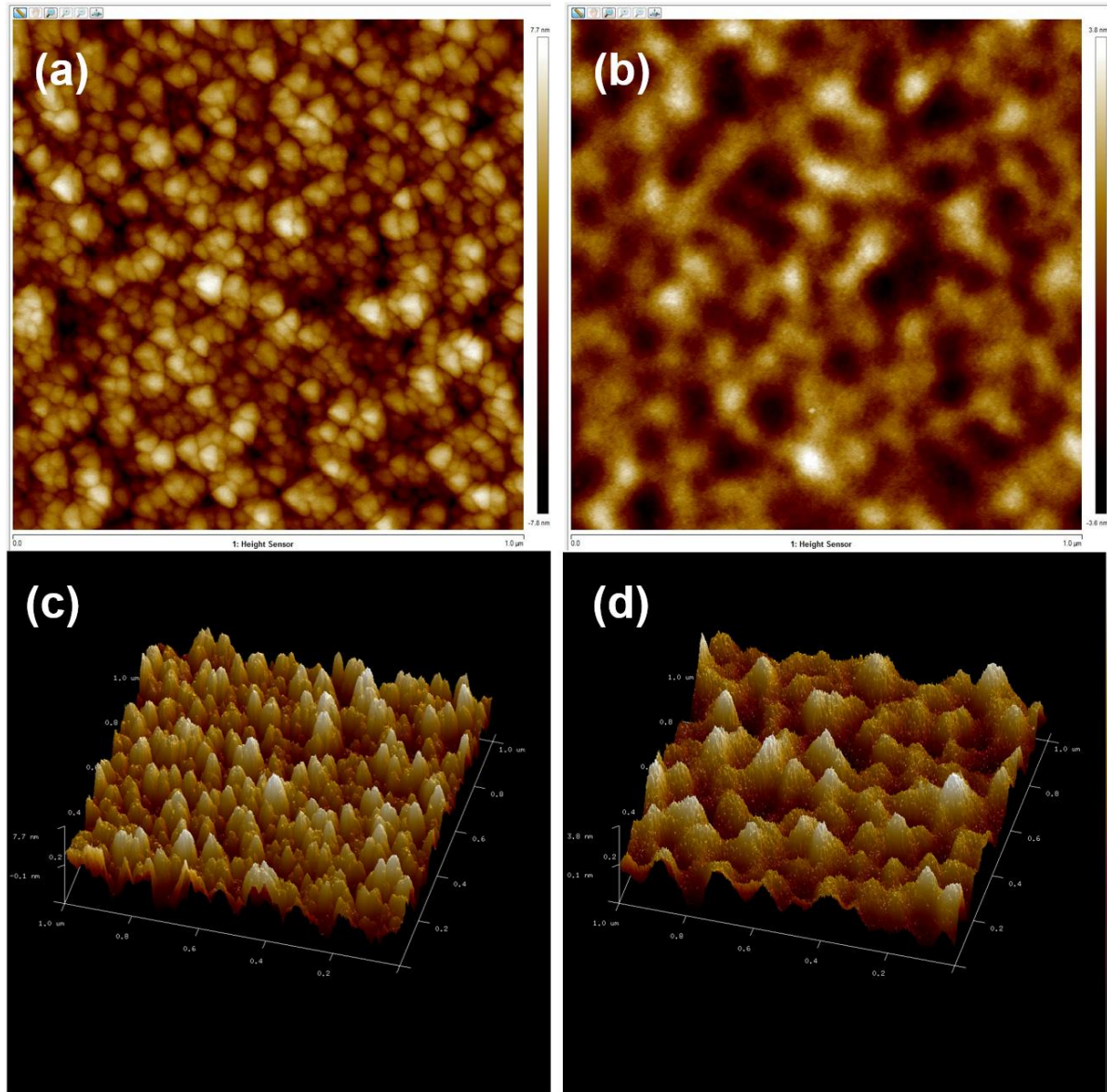


Figure 2-9 (a) 2D AFM image of 691 nm thickness PECVD with no treatment; (b) 2D AFM image of 691 nm thickness PECVD with 90 s Ar + N₂ plasma treatment; (c) 3D AFM image of 691 nm thickness PECVD with no treatment; (d) 3D AFM image of 691 nm thickness PECVD with 90 s Ar + N₂ plasma treatment

For PECVD oxide, only wafer-to-wafer bonding is conducted. 3 μm thermal oxide and 690 nm PECVD oxide were bonded in the vacuum wafer bonder (200°C, 1 hour). Also, 690 nm of

PECVD oxide were bonded to 690 nm of PECVD oxide. Both two bonding obtain relatively strong bond (cannot be sheared off manually). Pull test or blade insertion needs to be done in the future.

Meanwhile, the hydrophilicity of the oxide surface is detected by measuring the contact angle. The results are shown below in Table 2-6.

Table 2-6 Contact angles of different samples

Oxide source	Surface treatment	Cleaning after surface treatment	Contact angle 1 (degree)	Contact angle 2 (degree)	Contact angle 3 (degree)	Contact angle 4 (degree)	Average contact angle (degree)
PECVD	as-deposited	-	9.9	8.6	12.8	13.5	11.2
	30 s Ar + H ₂ plasma (45W)	no	51.5	50.1	54.1	51.2	51.7
		Ultrasonic bath	45.2	46.1	43.8	47.3	45.6
		Rinsing	41.9	39.4	45.1	43.2	42.4
	120 s Ar + H ₂ plasma (45W)	no	45.9	44.2	51.1	47.4	47.2
	30 s Ar plasma (100W)	no	58.7	55.6	57.8	57.8	57.5
		Ultrasonic bath	45.1	45.6	41.4	40.1	43.1
	60 s Ar plasma (100W)	no	56.4	55.3	56.7	58.2	56.7
		Ultrasonic bath	50.7	50.6	50.0	51.3	50.7
	30 s O ₂ plasma (100W)	Rinsing	36.5	29.9	22.4	31.8	30.2
thermal	as-grown	-	27.8	26.4	36.7	33.1	31
	30 s Ar + H ₂ plasma (45W)	no	56.9	54.6	54.3	53.5	54.8
		Rinsing	40.4	40.5	41.4	36.2	39.6
	Piranha clean	Bubble rinsing + spin dry	35.4	31.6	43.2	39.6	37.5
		Rinsing + blow dry	39.4	33.7	41.1	37.4	37.9

As can be seen, the as-deposited or as-grown samples have the lowest contact angles. Any kinds of surface treatment could enable the surface more hydrophobic. Based on the promising bonding results of thermal oxide with Ar/ H₂ plasma treatment and without post-cleaning (Figure 2-7), the average of 54.8-degree contact angle indicates that relatively hydrophobic surface is good enough for the oxide fusion bonding, and thus the surface treatment done on the PECVD oxide should not be the detractor of the bonding.

CHAPTER 3 STUDYING OF ELECTROCHEMICAL DEPOSITION NON- UNIFORMITY EFFECT ON DISHING DURING CHEMICAL-MECHANICAL POLISHING (CMP)

3.1 Introduction of the non-uniformity effect

In the last chapter, good fusion bonding of thermal oxide is obtained, but the bonding of PECVD oxide is still under investigation. Before any actual hybrid bonding experiment is conducted, simulation work is necessary to be done first. In this chapter, the process window for D2W hybrid bonding is attained using the Finite Element Analysis (FEA) simulations. The bonding strength gained from chapter 2 was used as the upper limit of simulation, and the complete touching of metal was applied as the lower boundary. The details of the modeling and simulation will be discussed in section 3.3.

D2W hybrid bonding consists of four steps: die/wafer fabrication, singulation, die tacking and batch annealing. These four steps will be elaborated in the following.

The first step is the die/wafer fabrication. In this thesis, the Damascene process[47] is used to obtain the pre-bonding surface. During the electrochemical deposition (ECD) process, either under-plating or over-plating might occur, as illustrated in Figure 3-1. Under-plating is unacceptable since the hollows at the center of pads/ vias are significantly larger than the dishing pits. Over-plating is therefore widely employed but this also results in a non-uniform film. The non-uniformity of the plating arises from nonuniform current density distribution. Although there are some approaches for better control of the uniform current density distribution during electroplating process[48]–[50], such as using wire beam electrode (WBE)[49] or multi anode baths[48], [50], this non-uniformity issue cannot be eliminated completely. For a typical Cu ECD bath (Technic Inc[51]), the non-uniformity across a 100 mm wafer is 5% -15%. This non-

uniformity effect is verified in our test vehicle which would be discussed in detail in the next section.

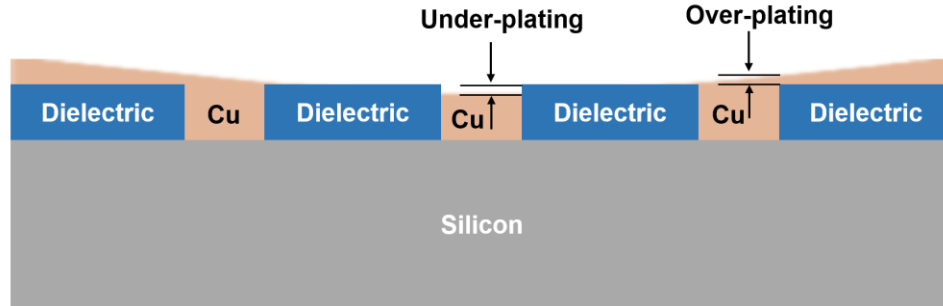


Figure 3-1 Schematic of under-plating and over-plating

The second step is singulation. Saw dicing, laser dicing and plasma dicing may be employed. Dicing may introduce edge generated particles as discussed in chapter 2 and needs to be addressed by cleaning.

The third step of hybrid bonding is the dielectric tacking at room temperature with weak Van der Waals force between dielectrics. Low temperature dielectric materials direct bonding has been investigated in the past decades[20], [52], [53]. The dielectric bonding experiment was conducted and discussed in Chapter 2 to get the effective bonding strength of SiO₂-SiO₂. Due to the stringent requirement of surface roughness and uniformity for the low temperature direct bonding, the thermal oxide with a very low surface roughness (R_{rms}=0.2 nm) was used to mimic the same thickness of PECVD oxide that was already CMP polished to attain an equivalent surface roughness before the optimized process of PECVD oxide bonding is achieved. As discussed in the Chapter 2, different surface treatment (O₂, Ar, and Ar/ H₂) was employed before tacking. Room temperature tacking with small external force then followed, and the bonded dies were annealed in a vacuum oven and were sheared to obtain the bonding strength.

The contacting silicon oxide area on a 2 mm × 2 mm die is 2.56e-6 m² (the mesa is 1.6 mm by 1.6 mm). Based on experimental data (Figure 2-6), the shear force of each die-to-wafer

bonding is larger than 200 N (O₂ plasma treatment was chosen due to higher bonding strength, and the more preferable Ar/H₂ plasma treatment need to be optimized). i.e.: the stress is 78.1 MPa. This value would be set as one of the boundary conditions in section 3.3.

The fourth step of hybrid bonding is batch annealing. In the last chapter, batch annealing is conducted to enhance the fusion bonding strength of dielectric materials. For hybrid bonding, batch annealing is also for metal expansion. Unlike TCB with the protruded metal bumps, the metal surfaces are recessed in hybrid bonding, which is essential to enable the dielectric surfaces to contact and tack first. Metal recess occurs naturally after the CMP process through the dishing effect. Hybrid bonding depends on the thermal expansion of metal to make the two metal surfaces mate and to be connected. The heating temperature is required to be sufficient to build the internal stress higher than the yield strength of metal, enabling the plastic deformation for stable bonding. Meanwhile, the temperature cannot be too high because the cumulative pressure between metal pads would unzip the bonded dielectric materials. Therefore, a suitable heating temperature window should be well established for void-free and reliable interconnection. Based on this perspective, a model is built to simulate the reasonable heating temperature window, which will be shown in section 3.3.

3.2 Experiment and results

The ECD non-uniformity effect is verified in our test vehicle. The fabrication process flow (cross-sectional view) is shown in Figure 3-2: 20 nm Ti/ 200 nm Cu seed layer was sputtered, and a Cu film was electro-plated on a 100 mm wafer. The thickness of Cu film varies from 0.8 μm to 4 μm . The wafer was then patterned to have squares of 1 mm x 1 mm. 150 mA DC current was employed, and different plating duration was carried out to get different plating thicknesses. The

fabricated test vehicle with the schematic of testing point is shown in Figure 3-3. Different locations across the wafer are labeled from a to i. The arrows labeled with Longitude (Lo) and Latitude (La) means that the thickness data is read as the sequence of “a-b-c-d-e” and “f-g-c-h-i” respectively. Both sequences are from one edge to center and then to the opposite edge.

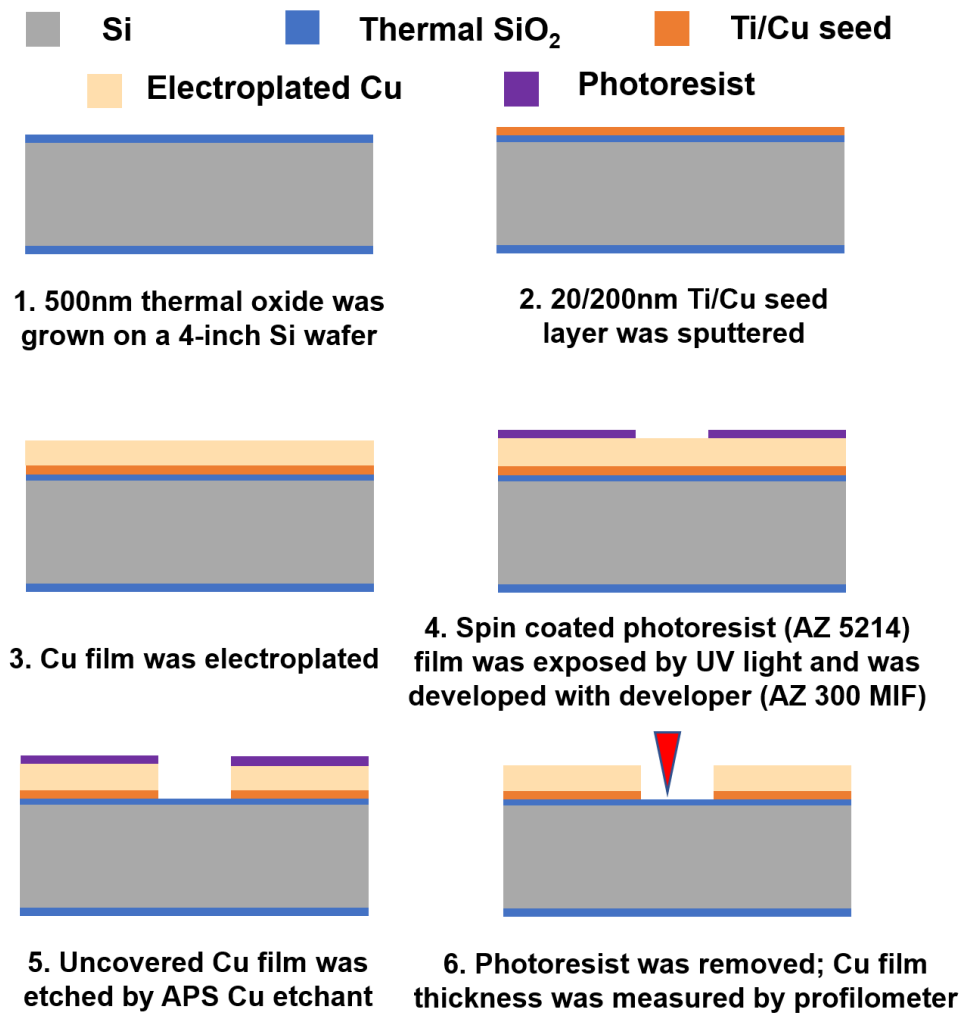


Figure 3-2 Process flow (cross-sectional view) of non-uniformity test vehicle

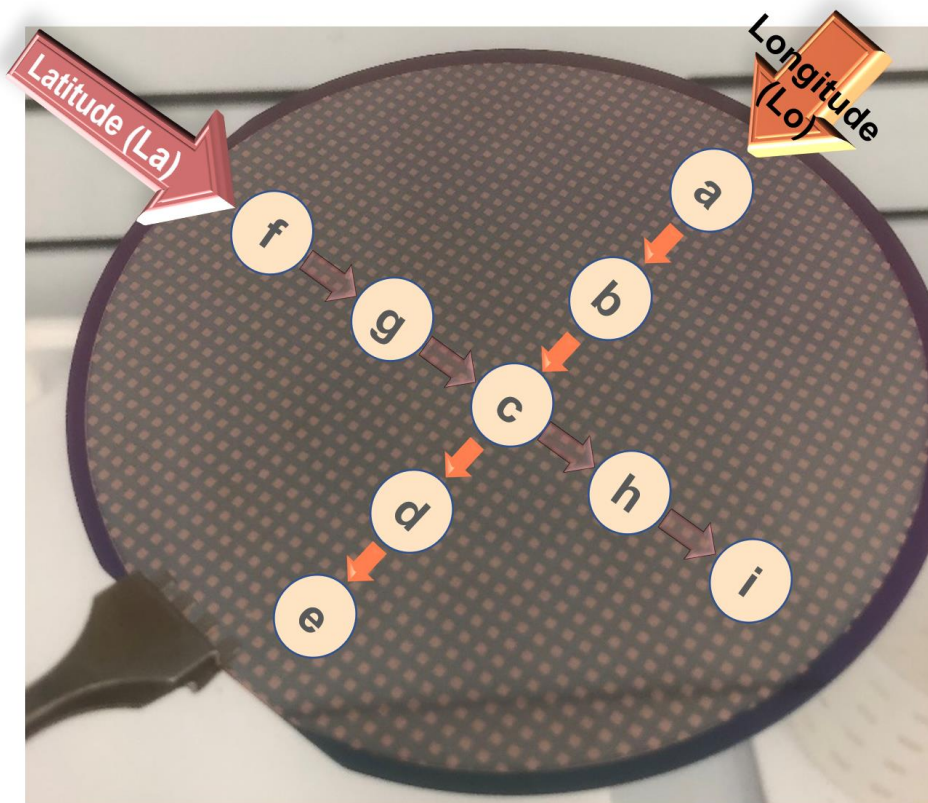


Figure 3-3 The fabricated non-uniformity test vehicle with testing points and data reading sequence

The thickness testing results are shown below in Figure 3-4. The label in the legend represents the plating time and data reading directions. e.g., 30 min (Lo) means that plating duration is 30 minutes, and the thickness data is read as the sequence of “a-b-c-d-e”.

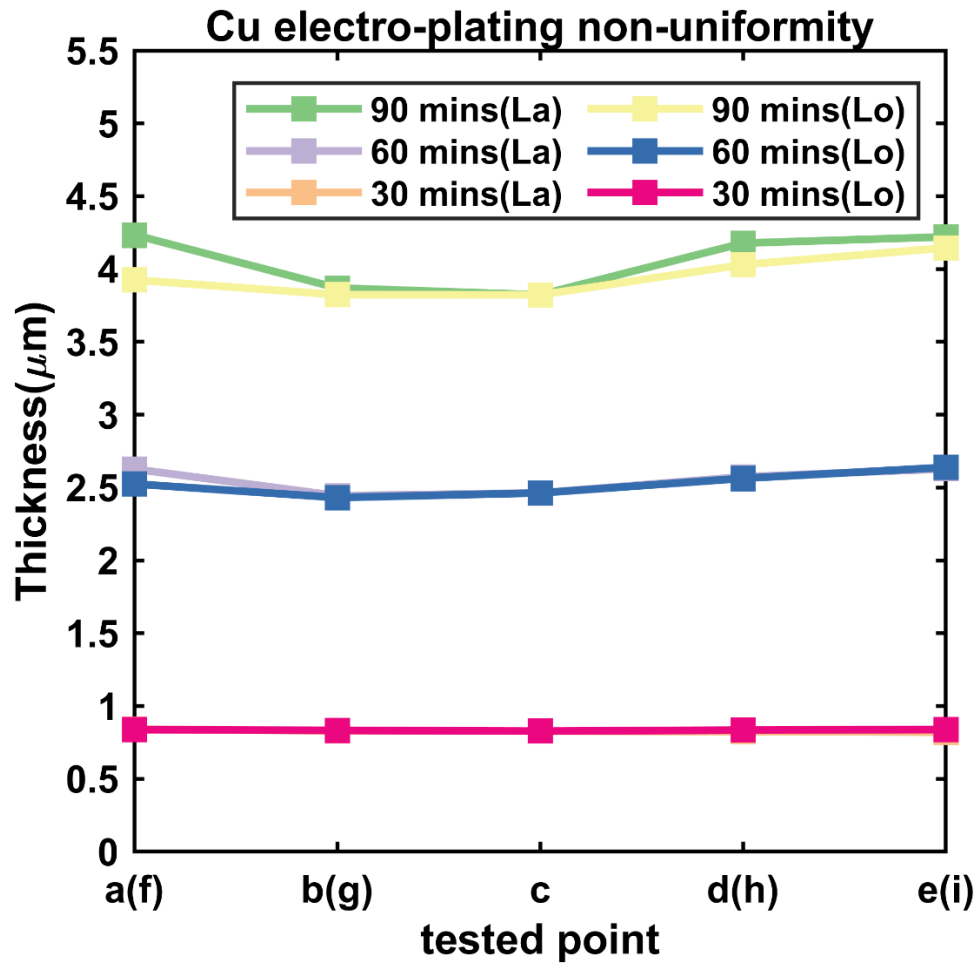


Figure 3-4 Non-uniformity across a 100 mm wafer using typical electroplating tool

According to Figure 3-4, for the Cu film with minimum 2.4 μm thickness, the non-uniformity from center (2.463 μm) to edge (2.639 μm) is about 6.6%.

The resultant uneven deposition is cumulative and then transferred to different dishing depth from the center to the edge of the wafer during the chemical mechanical planarization (CMP) process. To verify this, a metal recess test vehicle was fabricated. The schematic (cross-sectional view) of process flow is shown in Figure 3-5.

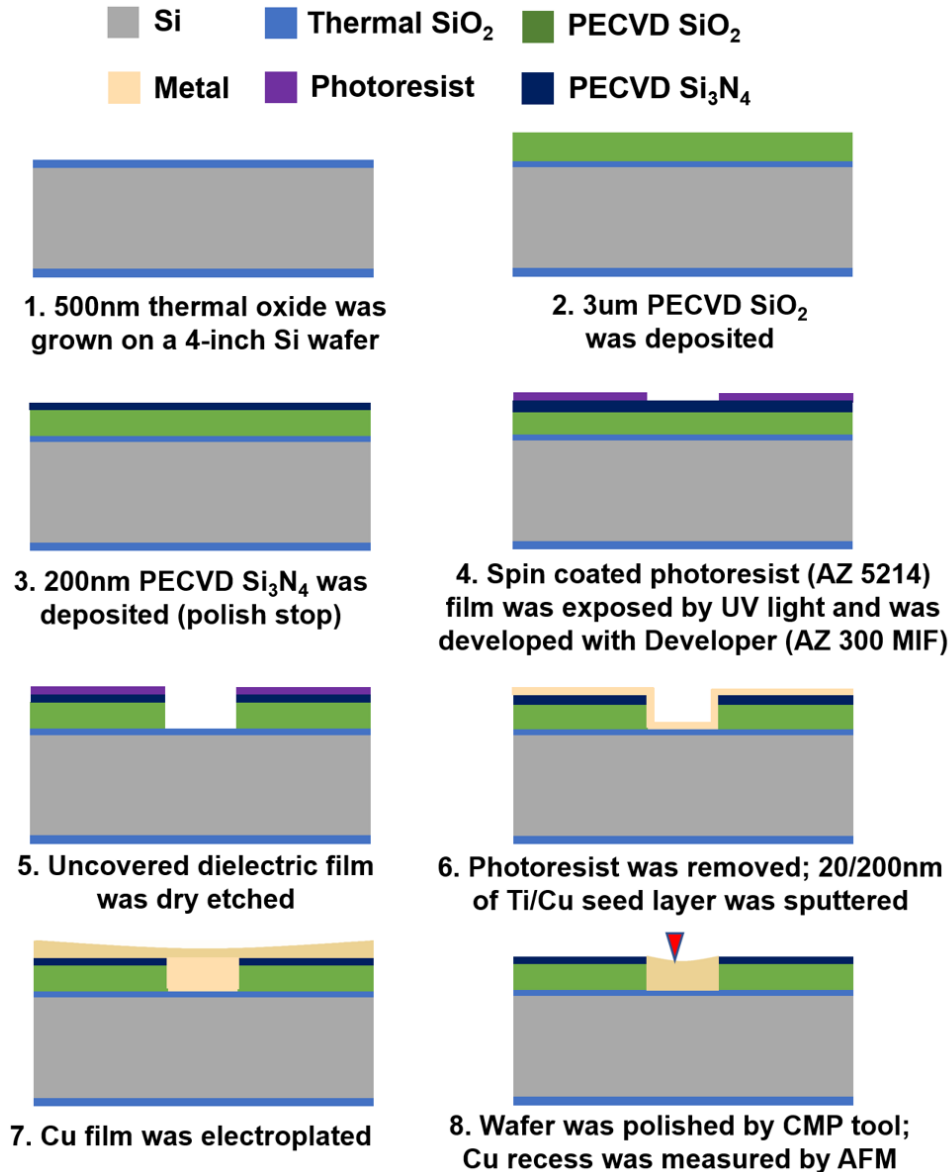


Figure 3-5 Process flow (cross-sectional view) of metal recess test vehicle

Atomic force microscopy (AFM) was used to measure the dishing depth across the wafer, and the results are illuminated below in Figure 3-6. The non-uniformity of metal ECD is observed to correlate to the non-uniformity of dishing depth. At the center of the wafer, thickness of deposited Cu film is the thinnest, which means the over-plated part at center will be removed completely earlier than that at the edge of the wafer. This causes more polishing duration of metal pads at the center, and the metal dishing is expected to be the most severe in this region. The largest

dishing depth within the test vehicle is obtained at the center of the wafer, which is 16 nm. The smallest dishing depth is 4 nm at peripheral of the wafer.

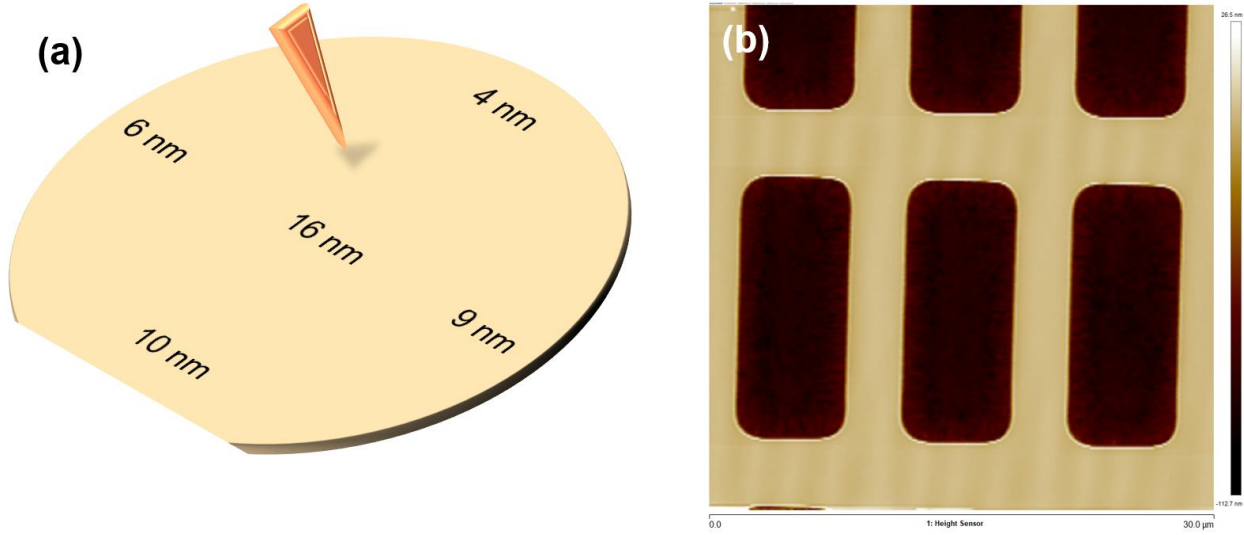


Figure 3-6 (a) Dishing distribution on a 100 mm wafer considering the non-uniformity of metal deposition; (b) Measuring metal pad dishing on wafer using AFM

3.3 Finite Element Analysis (FEA) setup and results

According to the experiments shown in the previous section, crucial problems of non-uniformity of dishing depths due to uneven ECD is considered here for developing a comprehensive model of hybrid bonding heating window. As previously mentioned, the temperature window is constrained: cumulative pressure should be less than the dielectric critical stress and the contact pressure of the two mating metal pads should be high enough to ensure good electrical connection. Note that during the annealing process, the dielectric bond strength is also improving. So, this is a very dynamic situation. In this section, the FEA model is built to gain insight into this process window for void-free and reliable interconnection.

To start with, the accumulated stress at bonding interfaces during the heating step for the frictionless metal-dielectric interfaces was calculated. 2D model was used for simplicity as shown

in Figure 3-7. CTE for thermal SiO₂ is typically 0.6 ppm, even for PECVD oxide the CTE is about 2.2 ppm, which are remarkably smaller than that of Cu (16.5 ppm). Therefore, in this model, the oxide was assumed not to expand so that the Cu is confined in 3 directions (interfaces 1,2, and 3 in Figure 3-7 below). The Cu surfaces are free at interface 4.

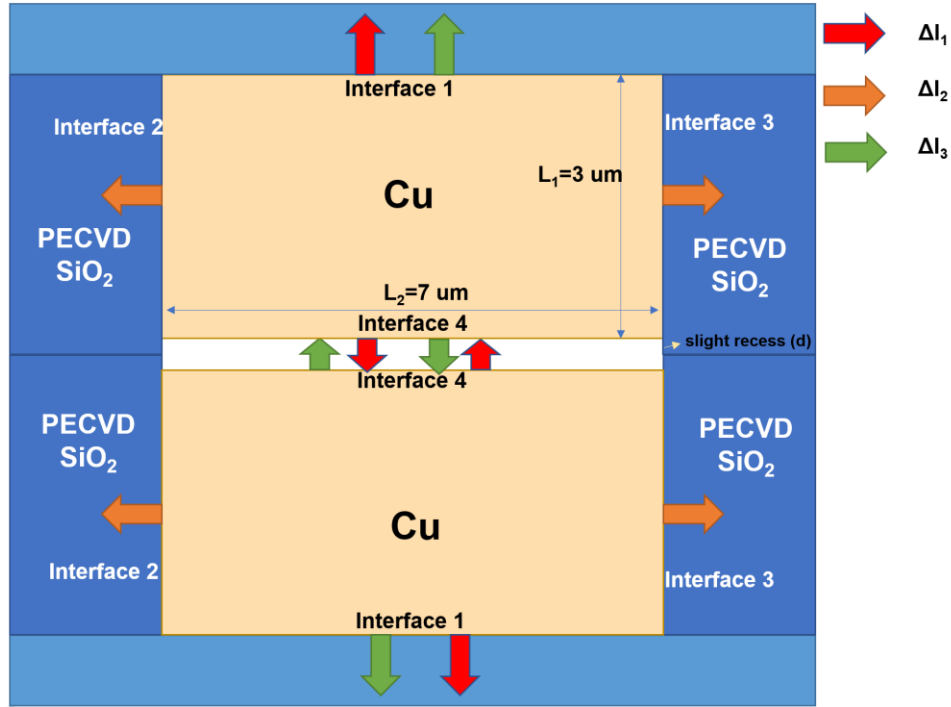


Figure 3-7 Schematic of Cu expansion

According to thermal expansion, Cu tends to expand and exert force on all four vertical and lateral interfaces. The resulting displacements are given by:

$$\alpha \Delta T = \frac{\Delta l_1}{L_1}, \quad \alpha \Delta T = \frac{\Delta l_2}{L_2} \quad (3.1)$$

Where Δl_1 is the vertical displacement, and Δl_2 is the lateral displacement. Since the interface 1 is confined, so the Δl_1 at this interface is virtual and convert to interface 4. Similarly, Δl_2 at interface 2 and 3 are also confined, so the tends to expand at these two directions convert to vertical displacements which are Δl_3 shown in the Figure 3-7. Again, Δl_3 at interface 1 is confined

so the displacement at interface 4 is required to be doubled. The total displacement at interface 4 equals to:

$$\Delta l = 2\Delta l_1 + 2\Delta l_3 \quad (3.2)$$

To calculate Δl_3 , Poisson's ratio is needed:

$$\gamma = \frac{\frac{\Delta l_3}{l_1}}{\frac{2\Delta l_2}{l_2}} \quad (3.3)$$

Where γ is the Poisson's ratio, $\frac{\Delta l_3}{l_1}$ is the transverse strain, and $\frac{2\Delta l_2}{l_2}$ is the axial strain at the interfaces 2 and 3 where stress is applied by the oxide. So, expression of Δl_3 is obtained:

$$\Delta l_3 = \frac{2\Delta l_2 \gamma l_1}{l_2} = 2\gamma l_1 \alpha \Delta T \quad (3.4)$$

If γ is taken as 0.32, α as 16.5×10^{-6} , and l_1 as $3 \mu\text{m}$, the expression of Δl can be written as:

$$\Delta l = (2 + 4\gamma)\alpha l_1 \Delta T = 1.62 * 10^{-10} \Delta T \quad (5)$$

If the heating temperature is 200°C , ΔT would be 170°C , and Δl would equal 27.6 nm . This value indicates the maximum effective recess amount. If the Cu pad is recessed less than 27.6 nm , the internal stress at the Cu bonding interface would arise. Using the Young's modulus of Cu as 120 GPa , the stress should be:

$$\sigma = E\epsilon = \frac{E\Delta l}{l_1} = \frac{E(27.6 * 10^{-9} - d)}{l_1} \quad (6)$$

Where d is the dishing value indicated in Figure 3-7. The relation between internal stress and the recess is plotted in Figure 3-8.

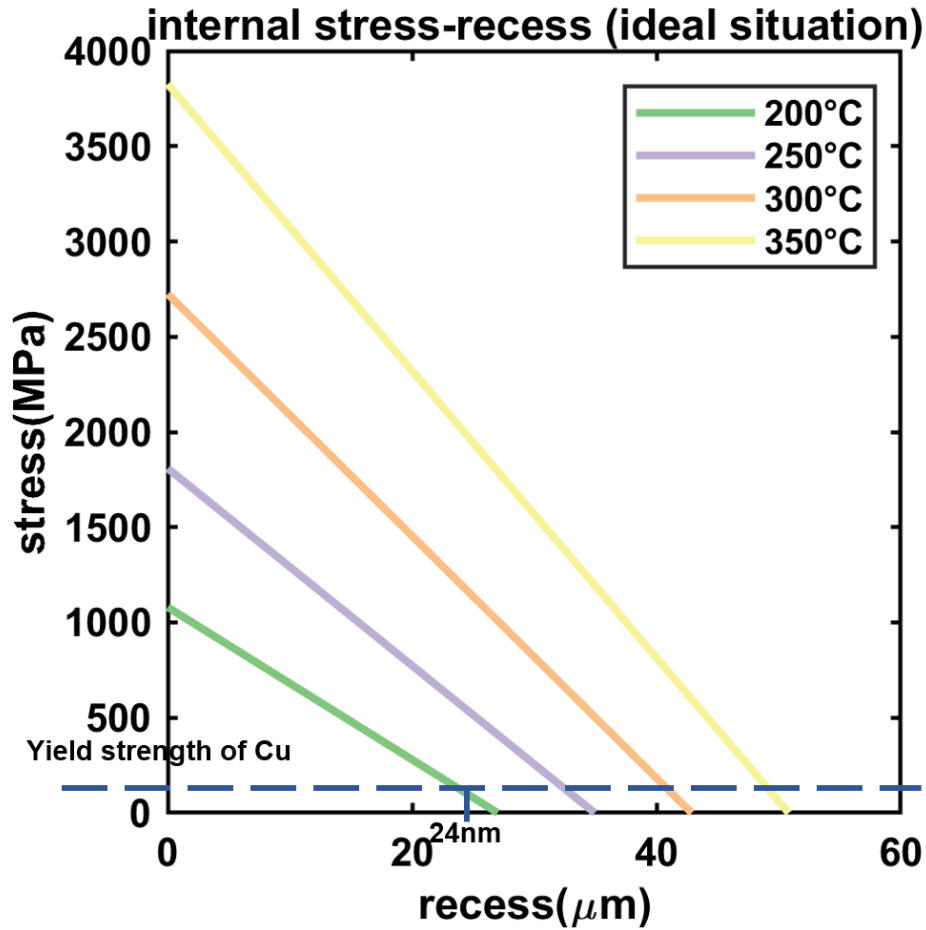


Figure 3-8 Calculation of recess vs. internal stress with frictionless metal-dielectric interfaces

Note that only elastic deformation is considered in this calculation for simplicity, but the stress is supposed to be saturated in reality due to the yield of metal. According to the calculation, when the accumulated stress is required to be higher than the yield strength, the recess should be less than 24 nm at 200°C. For the real situation, the interface boundary should be confined to some extent because of the existence of liner material, so the maximum recess should be less than the ideal value (24 nm at 200°C). Therefore, 4 nm- 16 nm was set as the simulation reference value for Cu recess. These values also correspond to the dishing depths which were obtained from Figure 3-6.

Two structures are discussed in the FEA of hybrid bonding as shown in Figure 3-9. The first structure is via to via bonding with 5 μm diameter. The metal dishing was generated with the

depth of 4 nm, 6 nm, and 8 nm. The dishing was assumed to be spherical cap[24], [26]. The second structure is pad-to-pad with shape of rectangular and size of $17\ \mu\text{m} \times 7\ \mu\text{m}$. The dishing was carefully defined with arcs along the median axes of Cu pad through which a Coons patch is fitted. The dishing depths at the center were set as 4 nm, 8 nm, 12 nm, 16 nm, respectively.

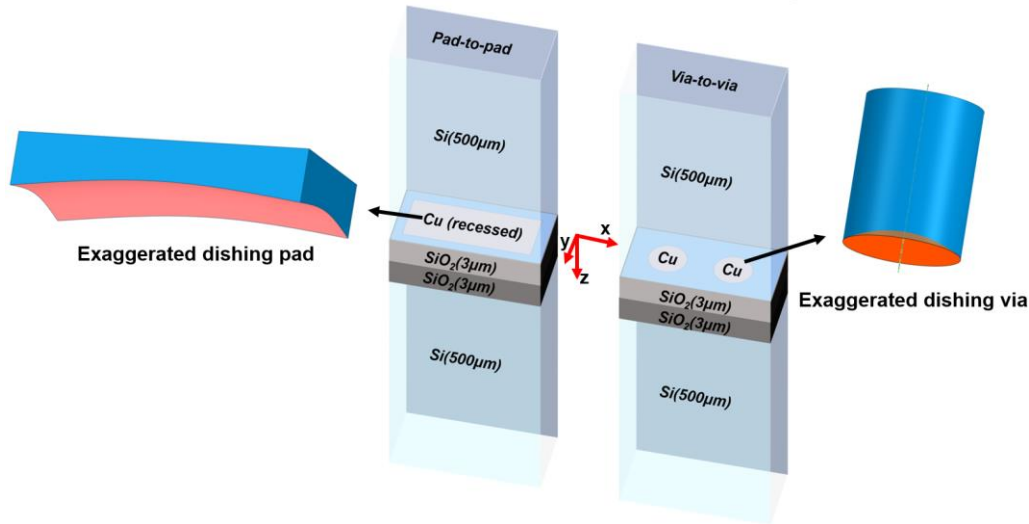


Figure 3-9 Schematic of Cu pads/ vias models, the bonding surfaces of Cu was recessed using simplified dishing models

With the changing of heating temperature, internal stresses on metal bonding interfaces and dielectric bonding interfaces were obtained. Based on these simulation results, the heating window for the typical D2W (wafer diameter: 100 mm) hybrid bonding was obtained, considering the non-uniformity of metal ECD.

3.3.1 Metal via- metal via model

The simplest situation with symmetries in the X and Y directions was first investigated. In this model, the cylindrical vias are embedded in the dielectric matrix. When the annealing temperature rises, the pistoning-effect of the metal expanding causes the two Cu surfaces make contact. The metal is constrained in the X and Y directions by the dielectric materials, and it expands only in the Z direction and eventually meets the Cu that is expanding from the other

surface. According to the simulation results of the stress on the metal bonding interfaces, when the edges of metal are under compressive stress (negative values, minimum point in Figure 3-10 (a)), the edge part of Cu via touches first. Once the edges of Cu surfaces contact, the hydrostatic pressure builds up. The Cu deforms plastically and bond to each other. Since the periphery of the Cu via bridges faster than the center, the void is most likely to occur at the center of Cu via when temperature is low enough (Figure 3-10 (a)). The maximum point locates at the center with positive value of stress (tensile stress) means the center of metal has not touched each other. Therefore, we should ensure that the expansion and stress on Cu via interface should be adequately high to guarantee the void-free metal bonding across the contact interface. At the very least, there should be compressive stress at the center of Cu bonding interfaces, which means the two surfaces contact and no nano-voids are left. The temperature when the stress at center of metal is larger than 0 was employed as the lower boundary of the heating temperature window.

According to the measured shear stress in Chapter 2, critical stress on dielectric is 78.1 MPa. When the tensile stress on dielectric material bonding interface is higher than this value, there is risk of dielectric unzipping, i.e., debonding. The average peeling stress on dielectric interfaces is calculated and compared with the critical stress. Thus, the critical stress was utilized as the upper boundary of the heating temperature window. For the purpose of this determination, we have not assume any improvement of the dielectric bond during the heating ramp up.

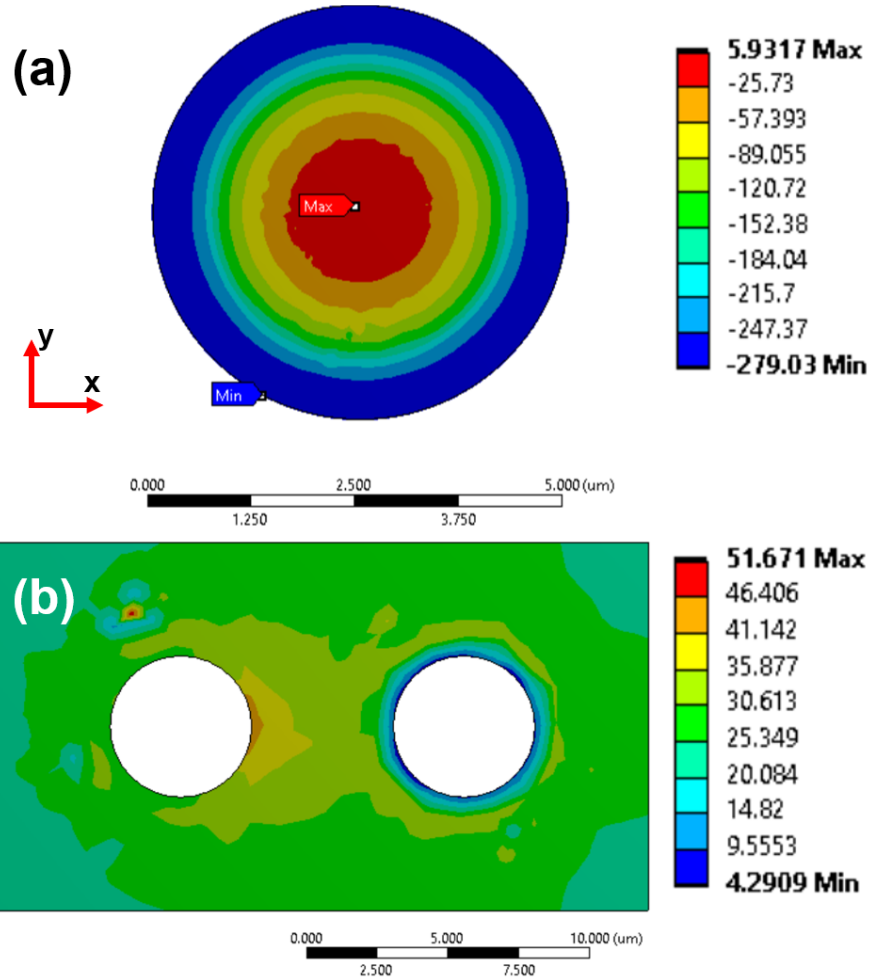


Figure 3-10 4nm recessed Cu vias are heated to 200°C: (a) Stress distribution at the mated Cu surface, center of the Cu vias with tensile stress (positive value) indicates risk of void formation; (b) Stress distribution at the bonded dielectric surface

The process window for different recesses of Cu vias is plotted in Figure 3-11. For $\Phi = 5$ μm vias: the annealing temperature should be $\geq 245^\circ\text{C}$ for 4 nm dishing, $\geq 260^\circ\text{C}$ for 6 nm dishing, $\geq 265^\circ\text{C}$ for 8 nm dishing.

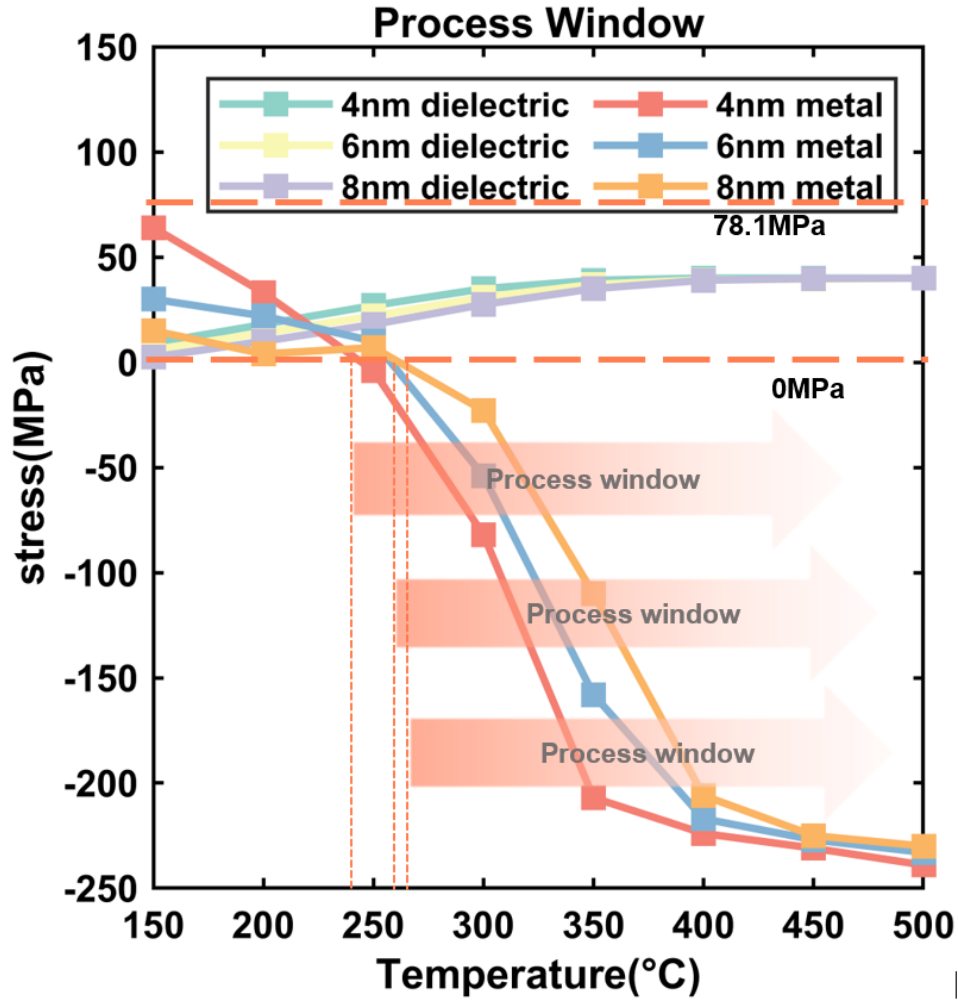


Figure 3-11 Process window for $\Phi = 5\mu\text{m}$ vias with different dishing depth: heating temperature should be adequately high to avoid voids formation

3.3.2 Metal pad- metal pad model

Rectangular pads with less symmetric in the X and Y directions are more often used for hybrid bonding. As mentioned in the experiment section, the non-uniformity of metal ECD causes the non-uniformity of dishing depth. This means the heating temperature window also depends on the distribution of recess values. Based on the recess data of metal after CMP, dishing values were set as 4 nm, 8 nm, 12 nm, and 16 nm. One example of simulation results with 4 nm dishing and 200°C heating temperature is shown in Figure 3-12. According to the simulation results, the short

edges, but not the pad center, are at highest risk for void formation. The lower boundary of process window is set to make sure this area on Cu with minimum compression stress (or maximum tensile stress) to touch while the upper boundary of process window was limited by the critical stress on dielectric (acquired from previous experiment data in Chapter 2), then the process windows for different dishing values can be predicted (Figure 3-13). For 4 nm/ 8 nm/ 12 nm/ 16 nm dishing, the process windows are 152°C-302°C, 248°C-310°C, 260°C-347°C, 295°C-390°C. Then these windows were utilized to set the exact process window for the 100 mm wafer based on the dishing distribution illustrated in Figure 3-6, i.e., the lower boundary for 16 nm dishing and upper boundary for 4 nm dishing were combined. The process window was obtained as 295°C-302°C.

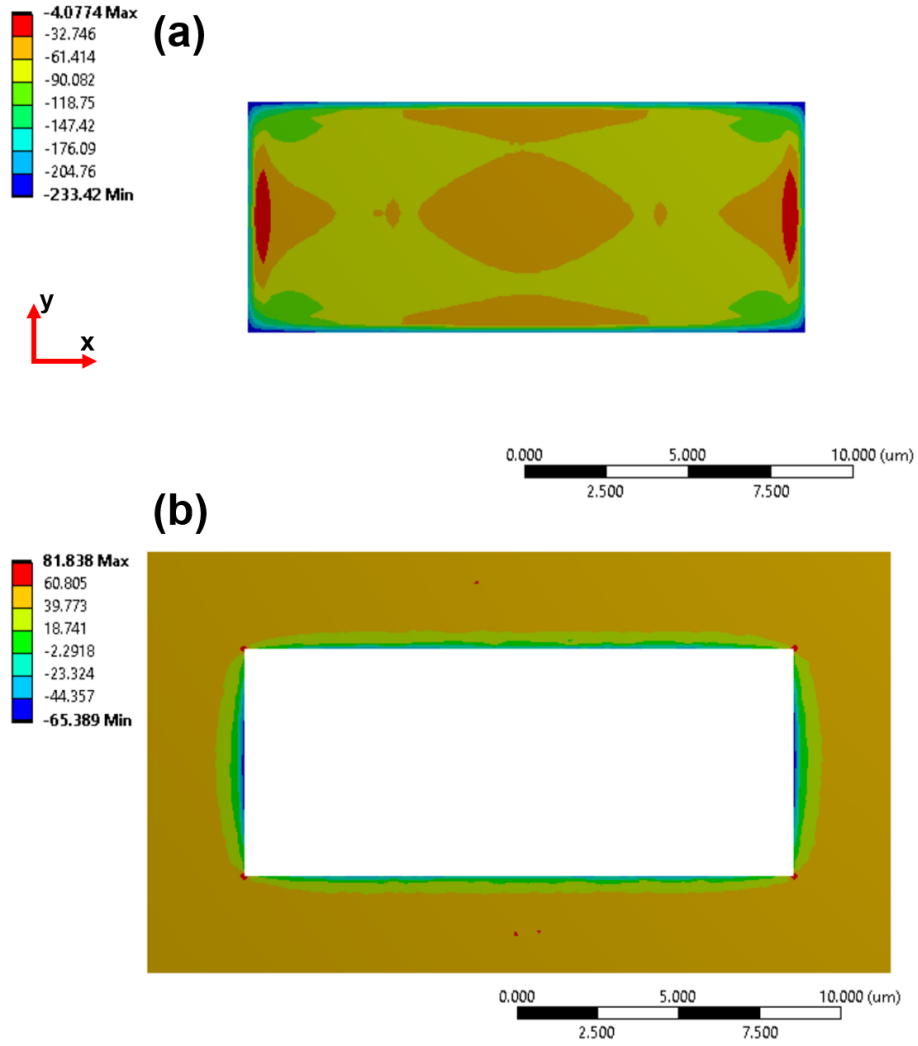


Figure 3-12 4nm recessed Cu pads are heated to 200°C: (a) stress distribution at the mated Cu surface, the two short edges of pad with low compressive stress indicates risk of void forming; (b) stress distribution at the bonded dielectric interface

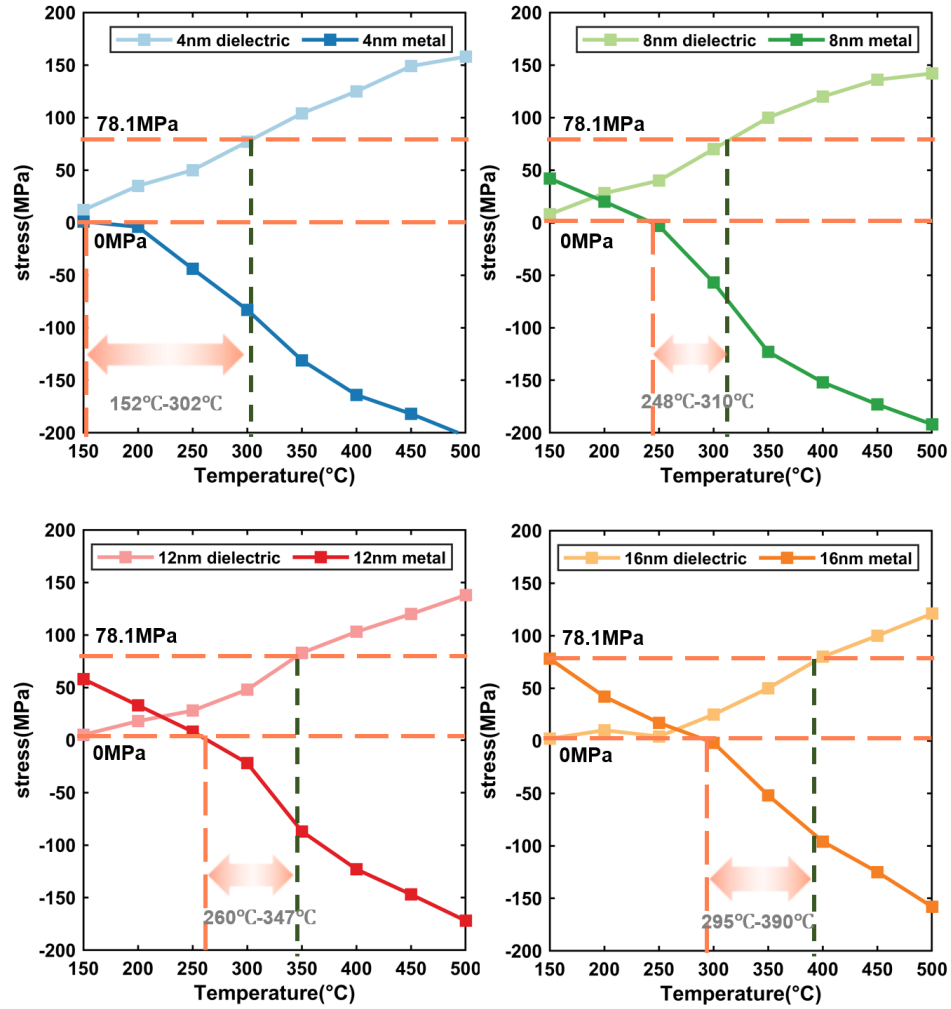


Figure 3-13 Process window for $17\mu\text{m} \times 7\mu\text{m}$ pads with different dishing depth: heating temperature should be in between of upper and lower boundaries to avoid voids forming in Cu bonding interfaces and to avoid dielectric material unzipping

CHAPTER 4 CONCLUSION AND PERSPECTIVE

In this thesis, die-to-wafer fusion bonding of thermal oxide was optimized, process of reducing the surface roughness and non-uniformity of PECVD oxide was also developed. Based on the thermal oxide bonding results, parametric investigations on D2W hybrid bonding are conducted. The FEA model is established to set up the process window with respect to temperature and dishing depth for void-free and robust D2W hybrid bonding by studying the internal stress on metal vias/pads and the peeling stress on dielectric bonding interfaces. The critical stress (78.1 MPa) of dielectric material gives the upper boundary of temperature, and the complete touching of metal limits the lower boundary. For 4 nm/ 8 nm/ 12 nm/ 16 nm dishing in rectangular metal pads, the process windows are 152°C-302°C, 248°C-310°C, 260°C-347°C, 295°C-390°C. Furthermore, the influence of the non-uniformity of metal electroplating (6.6% from the center to the edge of the wafer) on dishing depths variation (maximum 16 nm at the center to 4 nm at the edge of the wafer) is also examined by employing metal thickness testing vehicles and dishing non-uniformity testing vehicles. Thus, a more accurate and narrow process window is achieved to provide a better understanding of D2W hybrid bonding.

Though the thermal oxide bonding was achieved, PECVD oxide bonding still remains to be improved. Real hybrid bonding is supposed to be conducted with the guidance of achieved process window using FEA modeling. During hybrid bonding, Cu needs to be chemical-mechanical polished off, thus the polish stop layer is needed on top of the silicon dioxide layer, and this polish stop layer has to be etched off before low temperature tacking. This etching process should be developed without affecting the Cu recess a lot. When the hybrid bonding process is optimized, the shear force of the composite hybrid bonded dielets will be studied and correlated to the material and process parameters.

In addition, there will always be misalignment. This in turn can cause Cu to diffuse into the oxide and cause long-term reliability issues. Note that unlike elsewhere, there is no diffusion barrier to prevent this from happening. Hence, time-dependent dielectric breakdown (TDDB) may occur. It is worthwhile for us to study this phenomenon and assess its severity. In further research, new methods will be developed to mitigate these issues. Hybrid bonding addresses many issues in heterogenous integration and promises to be an important component of advanced packaging.

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